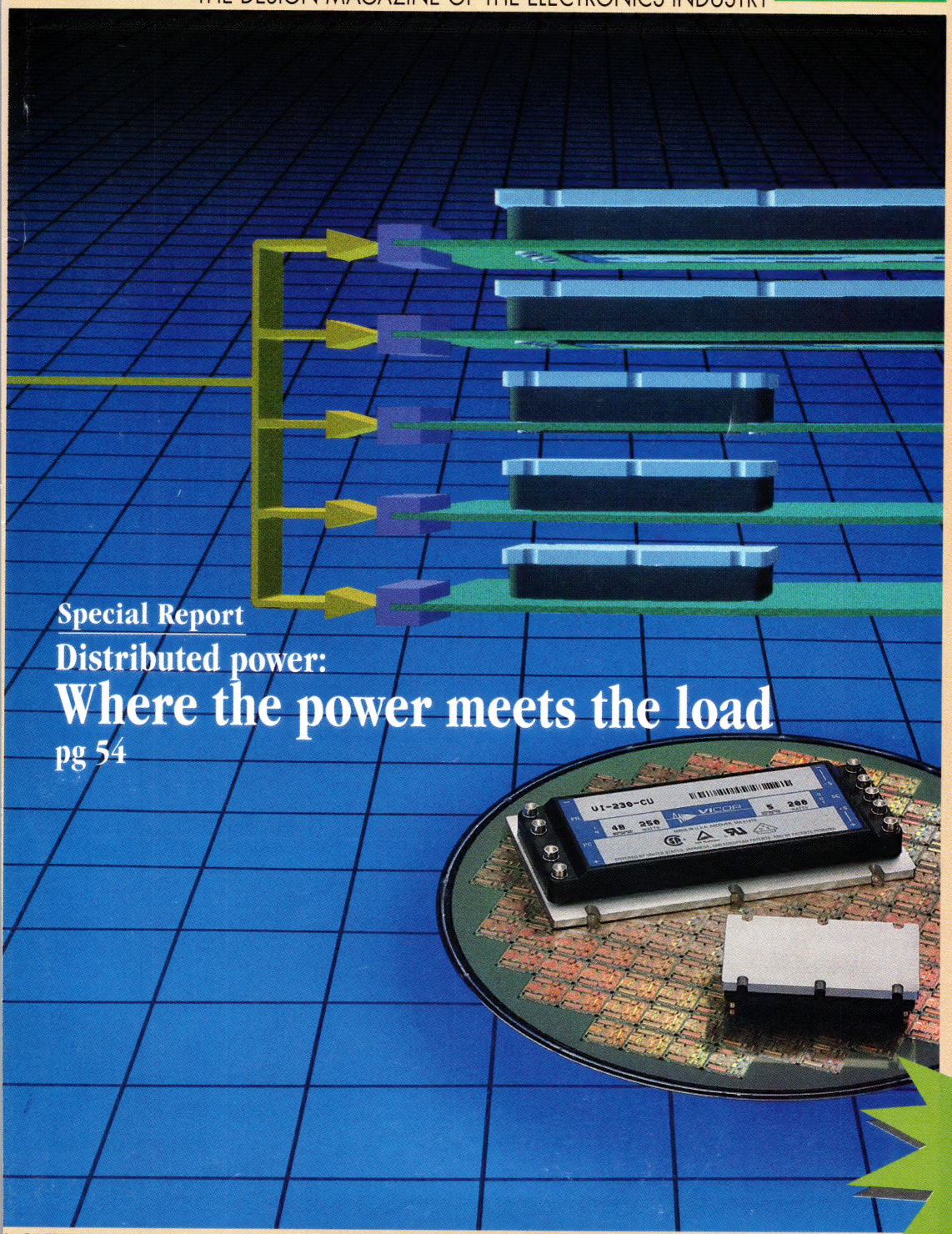
# EDN®

THE DESIGN MAGAZINE OF THE ELECTRONICS INDUSTRY

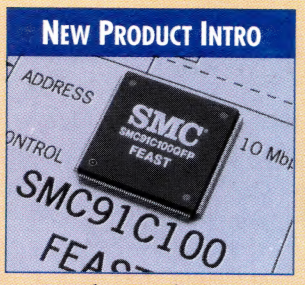




Special Report

## Distributed power: Where the power meets the load

pg 54

**NEW PRODUCT INTRO**




100-Mbps Ethernet sees silicon pg 115

April 28, 1994

**TECHNOLOGY UPDATES**



**DESIGN FEATURES**



See pg 133 for details of the Philips/EDN Dream Machine design contest

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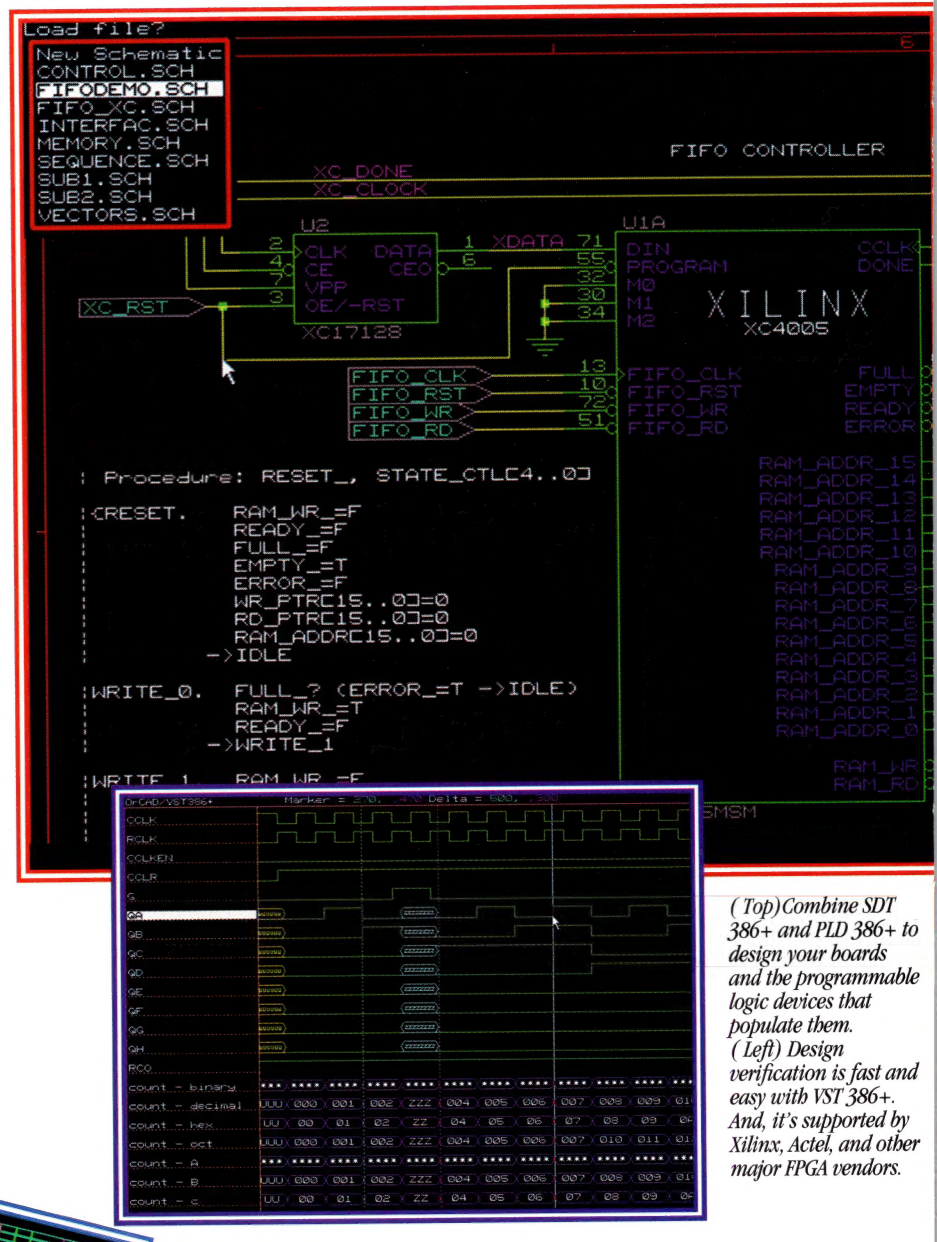





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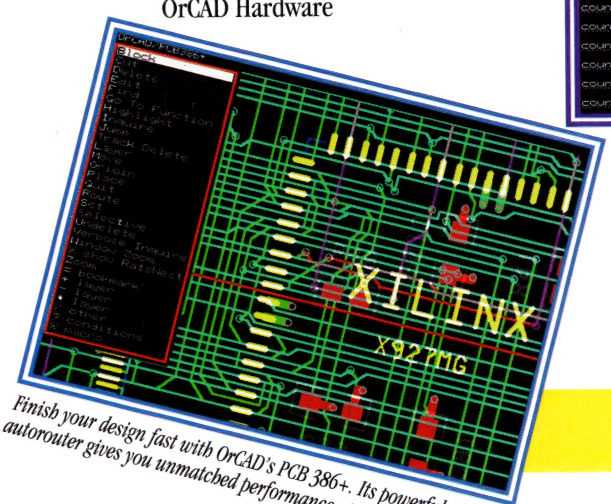


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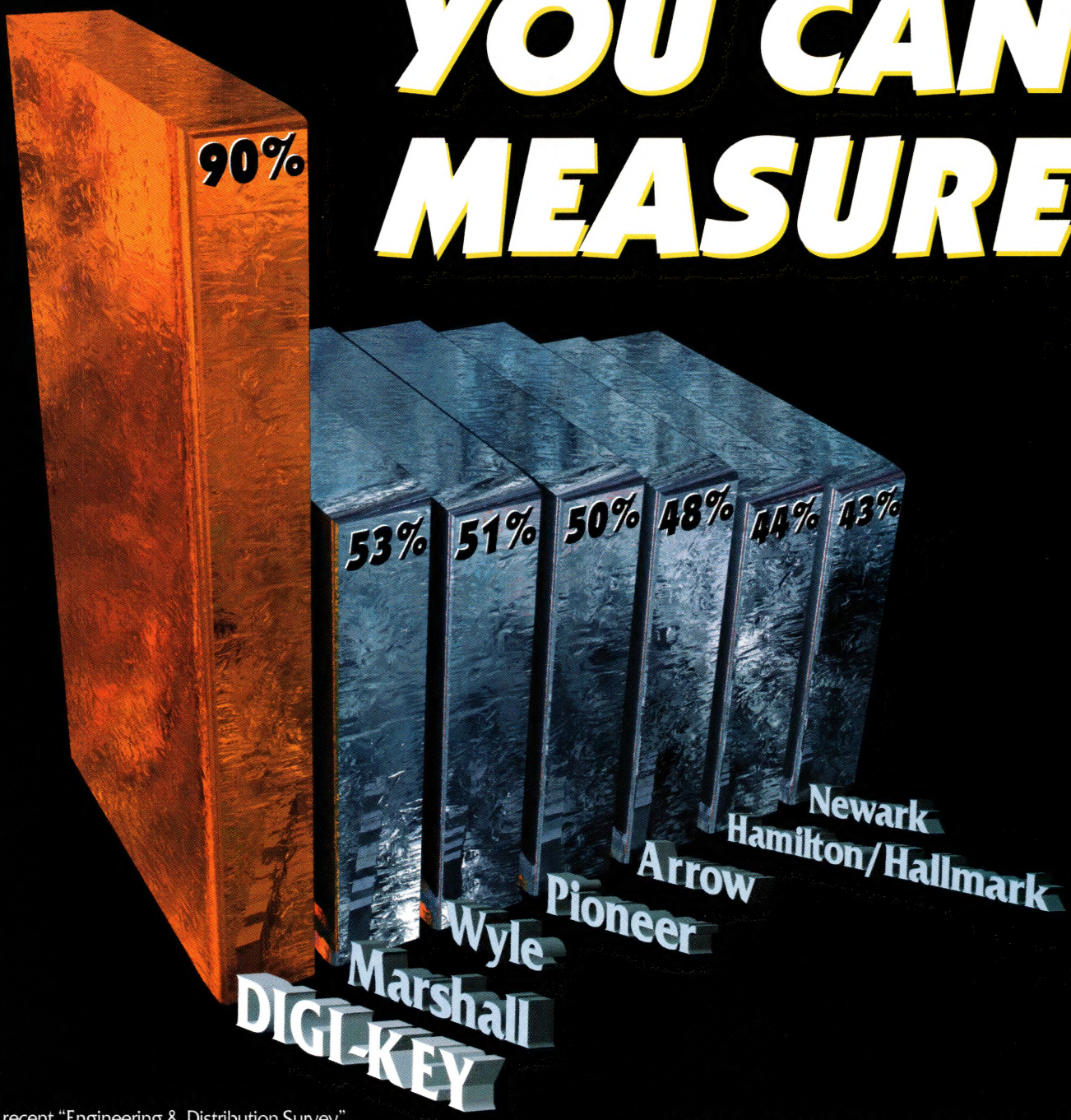


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Note: Since the bases varied for each distributor, direct comparisons should not be made.

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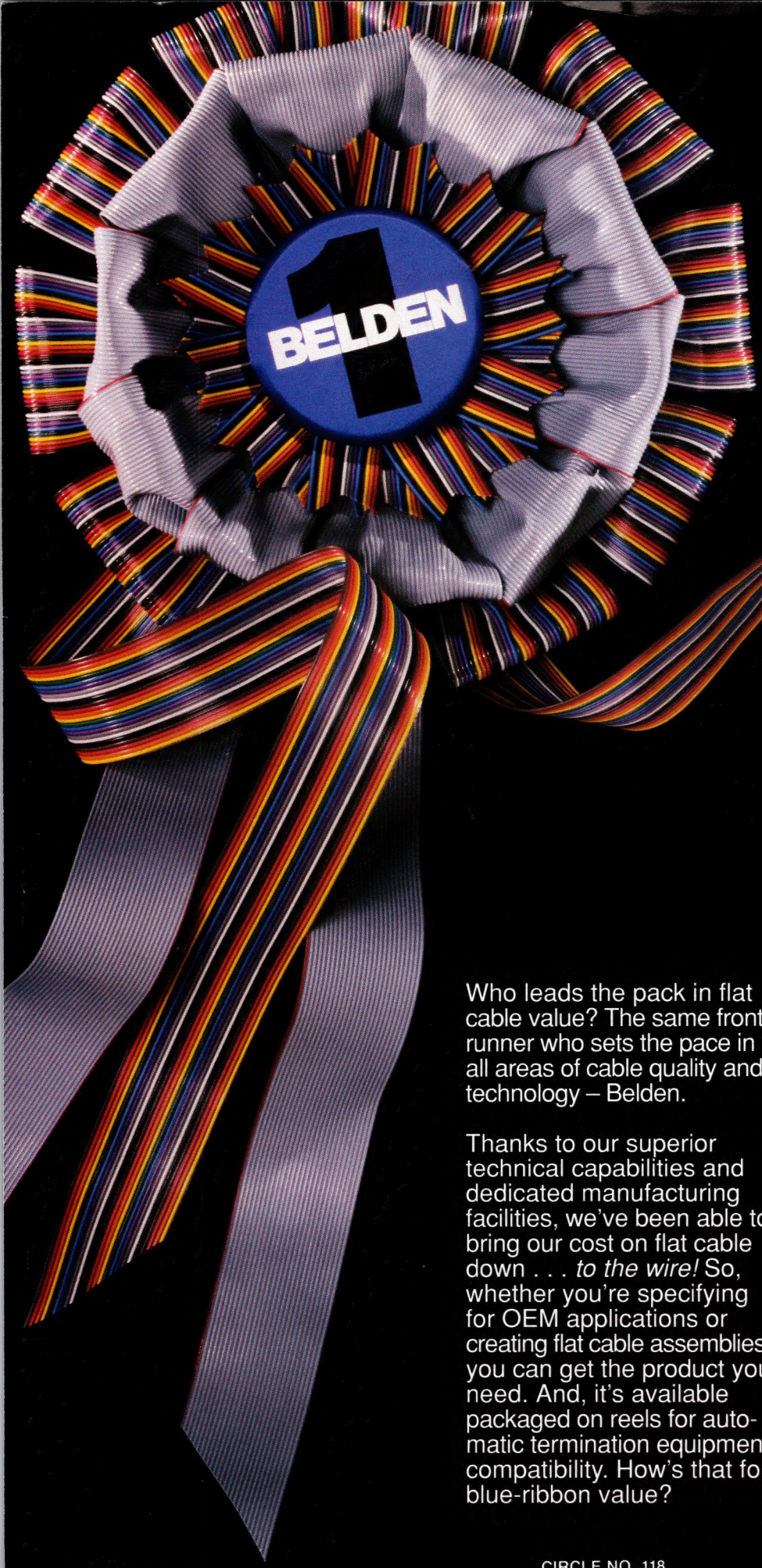


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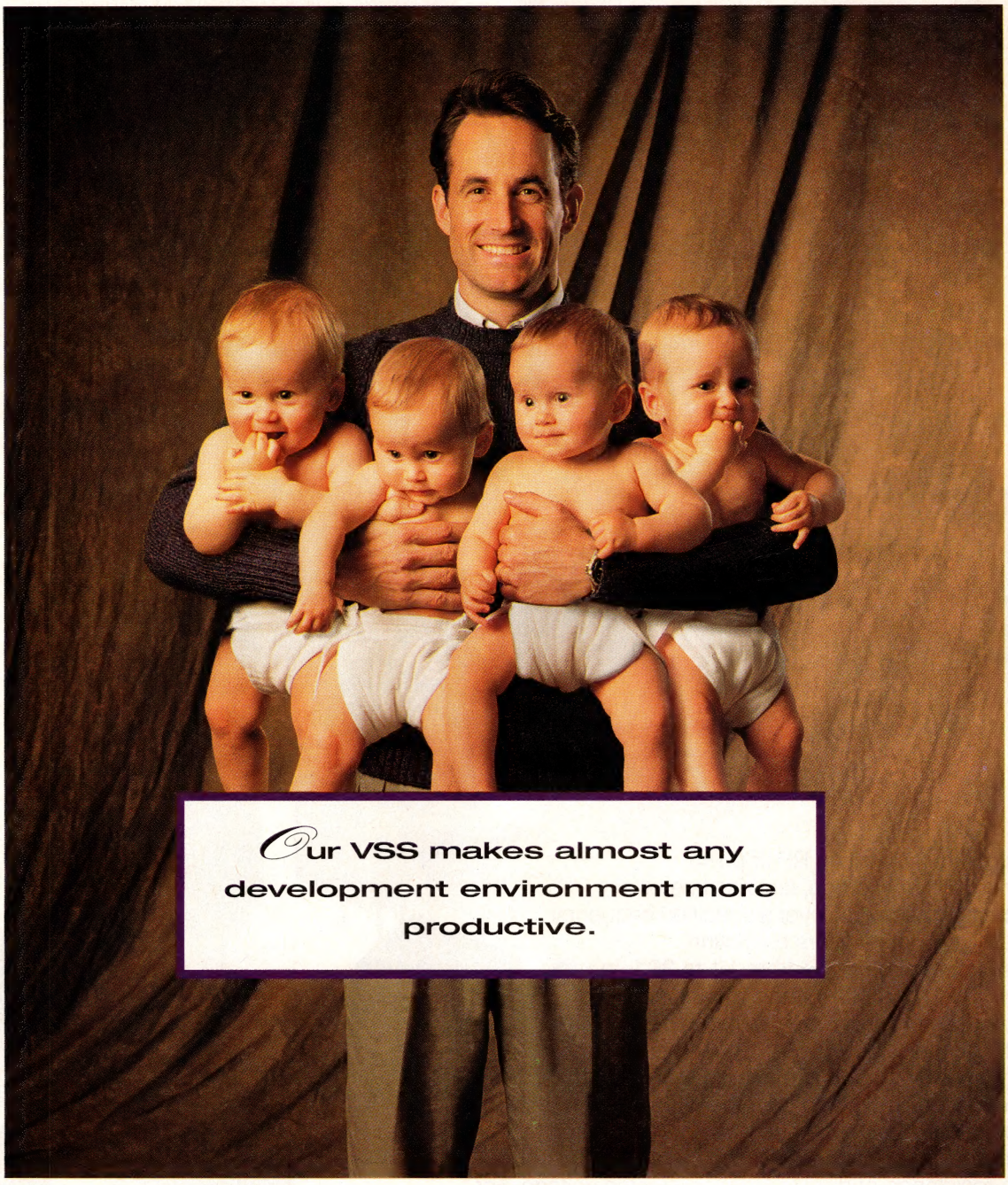


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April 28, 1994 VOLUME 39, NUMBER 9

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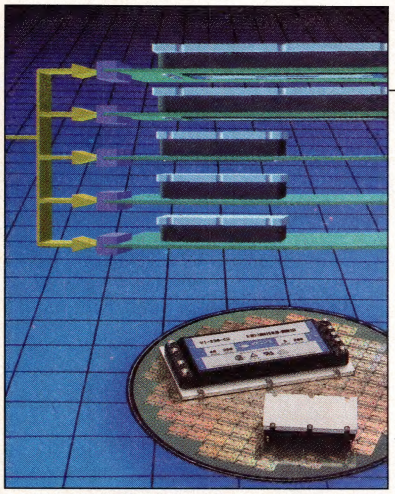

**On the cover:** Digital systems—regardless of size—are finding the benefits of distributed power too attractive to ignore. See our Special Report, beginning on pg 54. (Photo courtesy Vicor)



## SPECIAL REPORT



## DESIGN FEATURES



*Continued on page 7*

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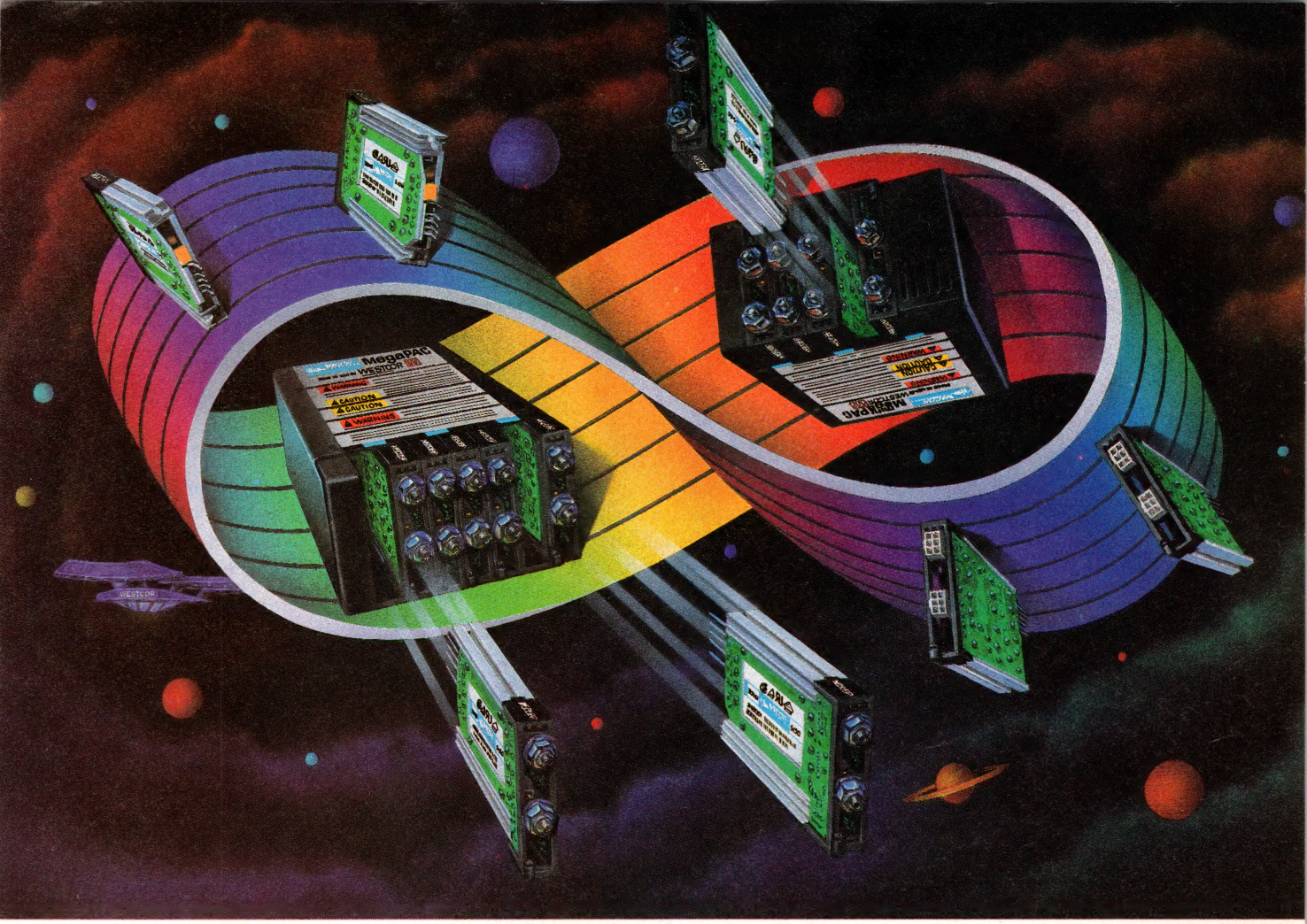

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EDN

April 28, 1994

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## Technology Updates



## Editorial



## New Products



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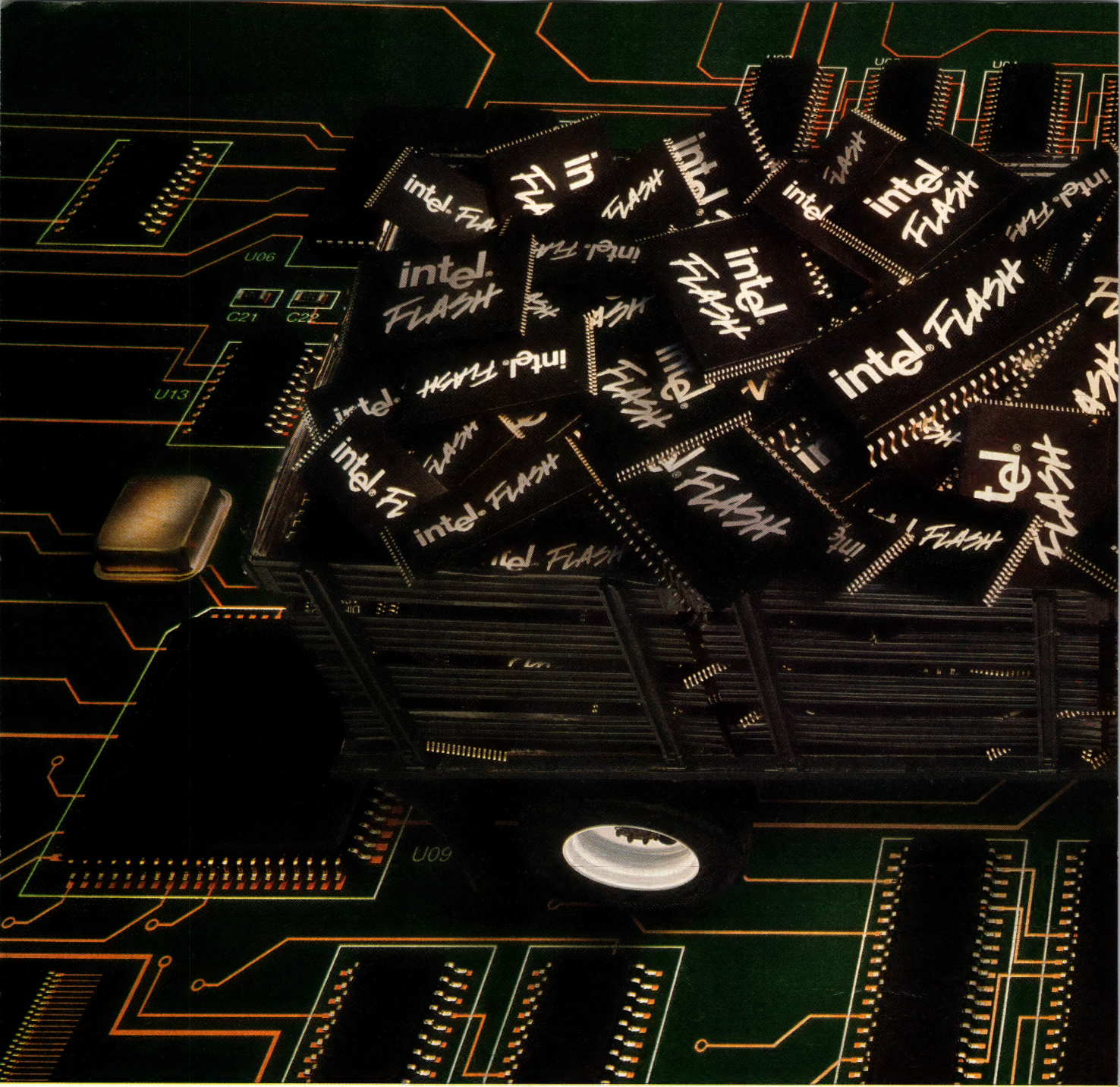


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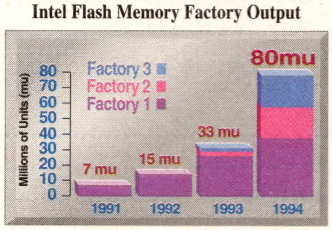
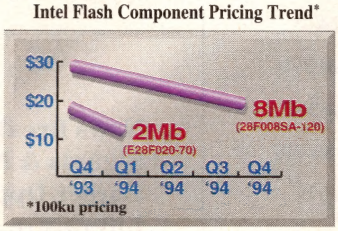
**Intel Flash Memory Factory Output**




**Intel Flash Component Pricing Trend***




 †Based on 9/93 Dataquest forecast of total flash units to ship in 1994.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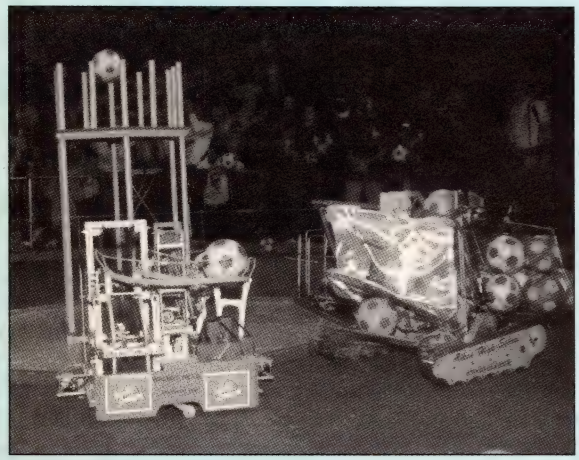
## Competition cultivates students' interest in engineering

In a competition to excite students about science and technology, a team of Procter & Gamble engineers and Walnut Hills High School (Cincinnati, OH) students recently won the US FIRST competition. Among the high-technology companies that joined with high-school students were AT&T Bell Labs, Boeing, Honeywell, NCR Microelectronics, Texas Instruments, and Xerox.

Before the contest, 43 teams of students and professional engineers had seven weeks to build a remote-controlled robot from a standard kit of parts. In each double-elimination heat, the robots had 2 minutes to score points by placing soccer balls of varying point values into two goals. Finals pitted the best four teams in a 2-out-of-3 format.



**The tall robot at left, built by a team of engineers at Procter & Gamble and students at Walnut Hills High School, won the third annual US FIRST design competition.**

Inventor Dean Kamen, recently voted Engineer of the Year by *Design News* magazine, founded US FIRST (For Inspiration and Recognition of Science and Technology). The annual competition is just one program the coalition sponsors to foster students' interest in technology. Circle the number below or contact the company for information on next year's competition.

—by Joan Lynch

US FIRST, Manchester, NH, (603) 666-3906. **Circle No. 480**

## Hardware and software bring data acquisition to Ethernet

Years ago, when Ethernet was new, few people expected it to become important in real-time data acquisition and control. That's because many thought Ethernet's CSMA/CD (carrier-sense multiple access with collision detection) protocol had data latencies so unpredictable that they ruled out using the technology where timing was critical. Although there still are some real-time applications you wouldn't trust to Ethernet, there are many in which Ethernet is quite fast enough. Moreover, the explosion in the use of Ethernet provides a compelling incentive to use it to get acquired data from industrial sensors to host computers; in most factories, you need look no further than a few feet for an Ethernet network to which you can connect your equipment.

Fluke Corp's NetDaq product line is ready to help you harness Ethernet for data acquisition. The hardware, which resembles a benchtop DMM (and will also be available in industrial enclosures), comes in two 20-channel varieties ($3995 for either one). The 2640A takes 100 readings/sec with 5½-digit resolution and 0.01% error. The 2645A takes 1000 readings/sec with 4½-digit resolution and 0.02% error. Both versions offer built-in signal conditioning that works with common types of transducers. The 2645A's solid-state multiplexer withstands common-mode voltages to 50V. The 2640's relay switches withstand 300V. In a demonstration, the NetDaq for Windows software that runs on the host PC ($1995 for use on a shared network; $1295 for use on dedicated networks) was impressive for its ease of use, both in setting up measurements and in displaying acquired data.

—by Dan Strassberg

Fluke Corp, Everett, WA, (800) 443-5853. **Circle No. 485**

## Board announcements spring from 68060 release

At least four manufacturers have announced plans to develop single-board VMEbus computers based on the recently released 68060 μP.

Motorola is among the first to release a 68060 board, the MVME177. The $4995 board uses a mezzanine bus to expand its memory capability and offers as much as 256 Mbytes of memory. It also includes SCSI-2 and Ethernet interfaces.

Another early entry comes from Heurikon Corp with its Nitro60 board ($5495). The Nitro60 mezzanine-bus structure allows for either memory or I/O expansion, depending on user needs. It also offers SCSI-2 and Ethernet interfaces. For more details on the Motorola and Heurikon boards, which will be available in June, see "Boards & Buses," pg 125.

In addition, Performance Technologies plans to create the PT-VME161, a single-board computer similar to the Heurikon Nitro60. General Micro Systems plans to create a 68060-based mezzanine card for its V64-60 computer board. The V64-60, a processor-independent design, accepts as many as three processors operating in parallel on its mezzanine cards. The Performance Technologies and General Micro Systems boards will be available at year-end.—by Richard A Quinnell

General Micro Systems Inc, Rancho Cucamonga, CA, (909) 980-4863. **Circle No. 481**

Heurikon Corp, Madison, WI, (608) 831-5500. **Circle No. 482**

Motorola Computer Group, Tempe, AZ, (602) 438-3287. **Circle No. 483**

Performance Technologies Inc, Rochester, NY, (716) 256-0200. **Circle No. 484**

## Logic analyzer price/spec war heats up

It's been less than a month since the last big logic-analyzer announcement. That one came from Tektronix. As so often happens when one of the test-and-measurement giants announces a new product, its archrival counters with a product intended to provide better specs at a lower price. You shouldn't be surprised, then, that Hewlett-Packard has announced a logic-analyzer plug-in that does 500-MHz timing analysis and 125-MHz state analysis and includes 1M frame of memory. The $13,500, 68-channel 16555A plugs into the 16500B logic-analysis system, whose $8800 mainframe accommodates five plug-ins with synchronized timebases (10 with an expansion chassis). A 204-channel configuration (including three 16555As) costs $49,300. By contrast, Tektronix's TLA 520 offers 400-MHz timing analysis and 100-MHz state analysis on 200 channels and a 14-in., high-resolution color display. Configured with 512k frames of memory, the TLA 520 costs $57,000.

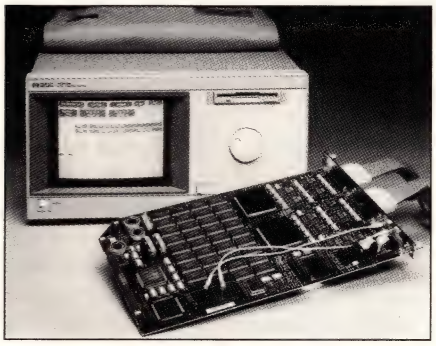
For over a year, HP has supplied 16500-series plug-ins that provide the same speed and others that offer the same memory depth as the 16555A, but the company hasn't had a plug-in that combines both features. A big advantage of the new configuration is that, unlike earlier deep-memory 16500-series plug-ins, the 16555A is compatible with hundreds of processor-specific pods and disassemblers (HP calls them inverse assemblers) that previously worked only with plug-ins limited to 8k frames of memory. The 16555A uses proven technology. It is based on a second-generation logic-analyzer chip that the vendor used in other 16500-series plug-ins and in its 1660-series portable analyzers. Owners of older 16500A mainframes can use the 16555A by installing a $4995 upgrade that endows the analyzer with 16500B capabilities.

Coincident with the 16555A announcement, HP is shipping two other enhancements to its logic-analyzer line: A high-density probing system makes HP logic analyzers and in-circuit emulators much easier to use with fine-pitch surface-mounted devices. An $1800 option for the 16500B provides enhanced networking, allowing full control of the analyzer from a networked workstation and replication of the analyzer's color screen in a window on the workstation's display.

—by Dan Strassberg

Hewlett-Packard Co, Santa Clara, CA, (800) 452-4884. **Circle No. 486**

Tektronix Inc, Beaverton, OR, (800) 426-2200. **Circle No. 487**



**Now you can have 1M-frame memory, as well as 500-MHz timing analysis and 125-MHz state analysis in HP's 16500B logic-analysis system. The 68-channel 16555A plug-in works with hundreds of processor-specific accessories that previously worked only with plug-ins limited to 8k frames of memory. The mainframe accommodates five of the plug-ins.**

## System combines signal generation with waveform capture and analysis

The VP8000 from TRW Business Intelligence Systems combines high-speed waveform capture (500M real-time samples/sec) with extraordinarily deep memory (to 64M samples), sophisticated analysis capabilities (including signal manipulation in time and frequency domains), and the ability to generate extremely long analog waveforms. A Unix workstation or a Macintosh Quadra can act as host for the VP8000, which comprises both hardware and software. The digitizer/memory/waveform-generation unit, which includes a NuBus slot, connects to workstations via a SCSI-2 port and to the Quadra via a NuBus interface. According to the vendor, either interface transfers data to host memory much faster than a DOS or Windows PC's ISA bus can. The unit can draw 10 1024-point waveforms/sec on the host's screen.

The vendor, which heretofore has designed and manufactured systems only for government applications—most of them classified—created a separate organization to design and market commercial products. The unit was designed from the ground up for commercial use, not adapted from a military design. Initial target applications are in verification of communications and medical-imaging-system hardware designs. The product sells for $50,000 to $90,000; it costs $55,000 with 32 Mbytes of memory and analysis software.—by Dan Strassberg

TRW Business Intelligence Systems, Sunnyvale, CA, (408) 752-2300. **Circle No. 488**

## Major vendor enters PC chip-set market

Samsung Semiconductor has entered the PC chip-set market with the introduction of its KS82C884 core-logic IC. The device includes cache, DRAM, and Video Electronics Standards Association (VESA) local-bus controllers and AT bus, keyboard, and peripheral interfaces within a single die. With data- and address-bus transceivers, the chip forms the core logic of a 486-based PC. The 3-chip set costs $14.25 (10,000). The KS82C884 chip set is the first in a family of PC-compatible chip sets planned by the manufacturer.

—by Richard A Quinnell

Samsung Semiconductor Inc, San Jose, CA, (408) 954-7000. **Circle No. 489**

## AccessBus gets keyboard support

AccessBus, a growing low-speed interconnection standard for desktop systems, builds on the I²C serial bus—now a common feature on many mainstream 8-bit microcontrollers. On the desktop side, Philips Semiconductor has added a key piece to AccessBus acceptance, the 8XC542. Built on the venerable 80C51, the keyboard controller integrates AccessBus, I²C, a PC ISA-bus interface, and an 8051 core.

The µC comes with 4 kbytes of ROM/EPROM, 256 bytes of RAM, two 16-bit timer/counters, and an AccessBus interface. The chip takes in key-

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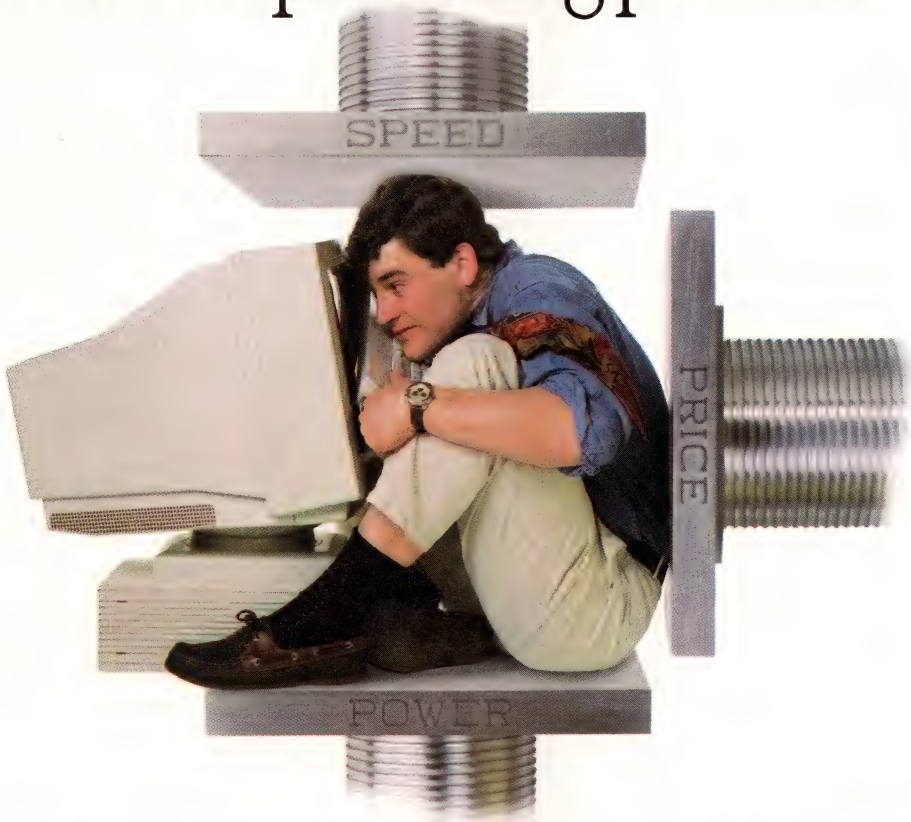


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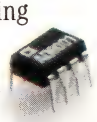


| Specification | AD8001 | CLC406 | HFA1105 | OPA623 |
|---|---|---|---|---|
| -3dB BW, G=+1, (MHz) | 800 | 160 | 300 | 340 |
| Peaking, G=+2, (dB/MHz) | .1/100 | .2/25 | .12/75 | .2/100 |
| Slew Rate (V/µsec) | 1200 | 1500 | 1100 | 2100 |
| Diff Gain/Phase (%/°) | .01/.025 | .02/.025 | .02/.02 | .12/.05 |
| Supply Current (mA, Max) | 5.5 | 6.7 | 6 | 4.5 |

ANALOG DEVICES

Analog Devices, Inc., Three Technology Way, P.O. Box 9106, Norwood, MA 02062-9106. Distribution, offices and application support available worldwide.

board, AccessBus, and mouse external interrupts and functions as a slave processor to a host CPU. The hardware can integrate into a PC ISA bus with a PC X86 host processor. Running at 16 MHz, the device has a maximum power supply current of 25 mA (active mode), 5 mA (idle mode), and 75 μA (power-down mode). The 8XC542 is available for sampling now, and production quantities will be available in June. It sells for $4.50 (25,000).

—by Ray Weiss

Philips Semiconductor, Sunnyvale, CA, (800) 234-7381. **Circle No. 490**

## FPGA density hits 25,000 gates

Shrinking device geometries have now taken field-programmable gate-array densities to 25,000 gates in the XC4025 from Xilinx. The company's earlier largest device, the XC4013, contains 13,000 gates. Xilinx fabricates the $654 (100) XC4025 with a 0.6-μm process. The device features 256 I/O pins and 1024 configurable logic blocks in a 32×32-bit array. The device shares architecture and features with other members of the XC4000 family. The company expects to push the IC's price down to around $400 (100) by the end of the year. It also plans to add a 40,000-gate member to the family by the end of 1995.—by Steven H Leibson

Xilinx Inc, San Jose, CA, (408) 559-7778. **Circle No. 491**

## 100VG-AnyLAN Forum promotes IEEE 802.12 technology

Several companies have joined to establish the 100VG-AnyLAN Forum (VGF) to promote the IEEE 802.12 technology for 100-Mbps Ethernet and token-ring networks. Current VGF members are AT&T Microelectronics, Hewlett-Packard Co, IBM, Optical Data Systems, Proteon, and Ungermann-Bass. Several other companies, including MultiMedia LANs Inc and Racore Computer Products, are planning to join the forum.

One of VGF's objectives is to provide an information-sharing forum for end users, resellers, system integrators, and vendors interested in 100VG-AnyLAN technology. The group also wants to support multivendor application development by providing general and technical information on the IEEE 802.12 standard. The forum plans to coordinate multivendor interoperability testing and certification at the University of New Hampshire, Durham, NH, with the leading network operating-system vendors, including Banyan, Microsoft, and Novell. Annual membership dues for VGF are $5000.

—by Fran Granville

100VG-AnyLAN Forum, North Highland, CA, (916) 348-0212. **Circle No. 492**

## SHORTS

**IEEE picks wireless LAN standard.** The IEEE 802.11 Standards Committee has approved a high-speed physical-layer option for wireless LANs. The option allows for frequency-hopping spread-spectrum communications using 4-level Gaussian frequency-shift keying (4GFSK). The initial proposal came from Proxim Inc, which makes wireless-LAN products based on the scheme. Proxim Inc, Mountain View, CA, (415) 960-1630. **Circle No. 493**

**Photon Dynamics enters joint-development agreement with USDC.** Photon Dynamics and the US Display Consortium (USDC) have announced an agreement under which Photon Dynamics will develop and demonstrate an automated flat-panel inspection system for use in the cell and module stages of flat-panel-display production. USDC, which includes the Advanced Research Projects Agency, AT&T, Tektronix, Xerox, and others, hopes to develop the US infrastructure to support a world-class US manufacturing capability for high-definition displays. Photon Dynamics Inc, Milpitas, CA, (408) 433-3922. **Circle No. 494**

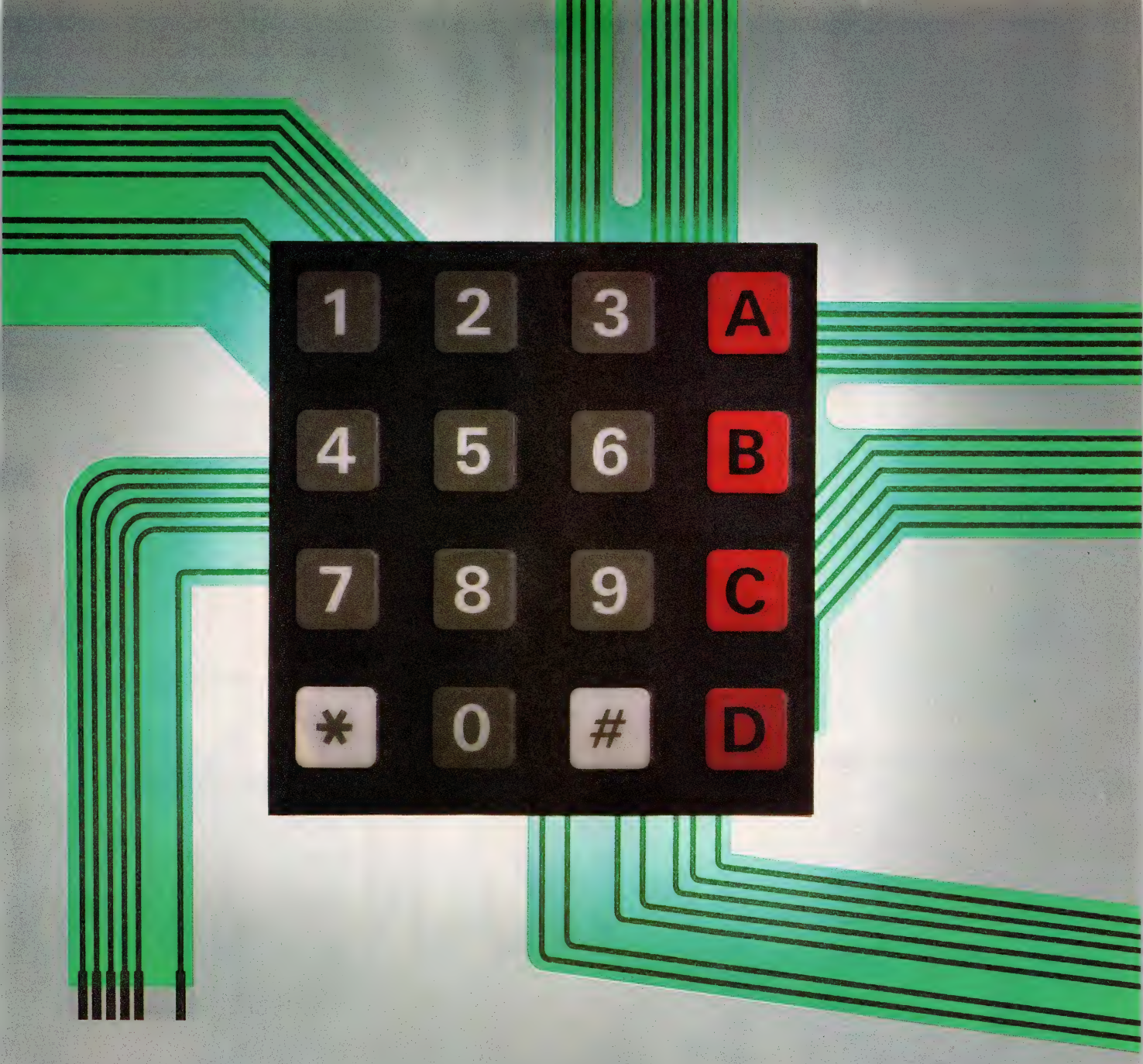
**Microwave breakfast.** If you're attending the IEEE's MTT-S International Microwave Forum in San Diego (May 22 to 27), stop by the Marina Ballroom E at the Marriott Hotel and Marina on Tuesday or Wednesday, May 24 or 25, for a free breakfast, courtesy of Mini-Circuits. You can pick up a free copy of the company's 740-pg Designer's Handbook at the same time. Mini-Circuits, Brooklyn, NY, (718) 934-4500. **Circle No. 495**

**Conference highlights DSP applications and technology.** DSP$^X$, a conference and exposition featuring more than 70 companies displaying DSP boards, devices, software, systems, workstations, and other hardware, takes place June 13 to 15 at the Moscone Convention Center in San Francisco. Sessions at the conference include three series: The introductory 100 Series includes tutorials, workshops, and introductory presentation; the more advanced 200 Series describes and compares DSP products; the advanced 300 Series offers technical-application sessions and case studies. DSP$^X$ Customer Service, Reed Exhibition Co, Stamford, CT, (203) 352-8289. **Circle No. 496**

**GE and Motorola to market lighting systems.** According to GE Lighting and Motorola Lighting Inc, electronics and key advancements in lamp technology are fueling a revolution in the lighting industry. The companies expect US market growth for electronic ballasts to be more than $2 billion by the year 2000. The companies will jointly market GE linear (tubular) fluorescent lamps and Motorola Lighting electronic ballasts as an energy-efficient light system. GE Lighting will initially market a line of co-branded GE-Motorola electronic ballasts manufactured by Motorola. The two companies also plan to collaborate in developing other new lighting products. GE Lighting, Cleveland, OH, (216) 266-8954. **Circle No. 497**

Motorola Lighting Inc, Buffalo Grove, IL, (708) 480-6842. **Circle No.498**

**Neural-network-modeling tool costs $199.** Vesta Services has announced Qnet Version 1.5 for DOS and Windows. The neural-network-modeling tool provides interactive training and recall modes, a connection editor for network customization, a graphing utility for interactive monitoring of network and training information, and automatic learning-rate control. Vesta Services Inc, Winnetka, IL, (708) 446-1655. **Circle No. 499**

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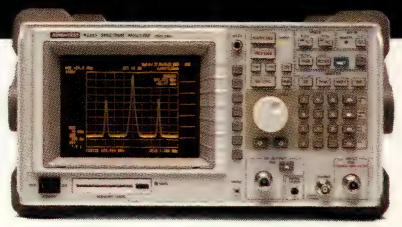

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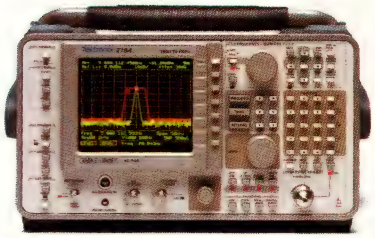

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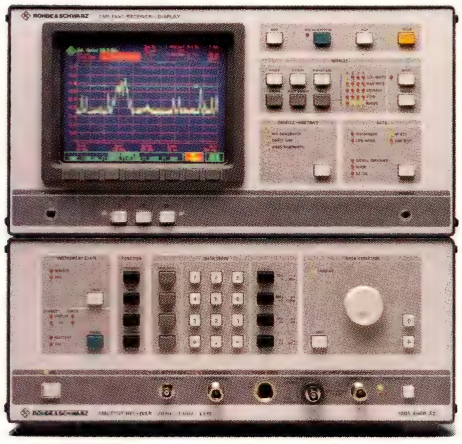

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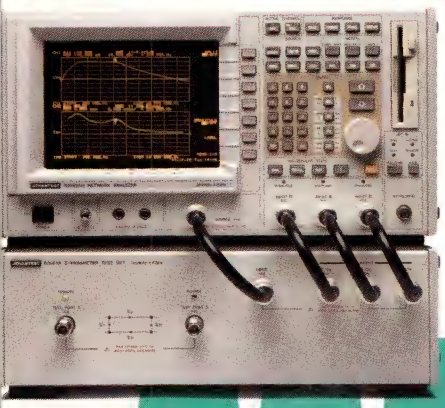

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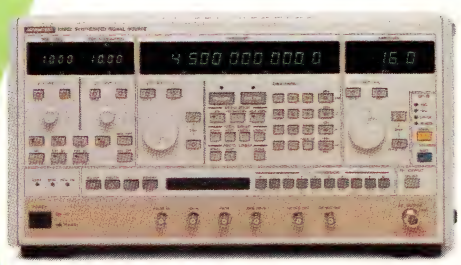

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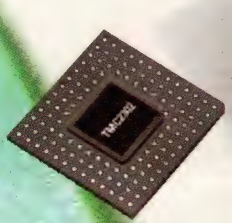



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CIRCLE NO. 38

## Diagrammatic-programming smoke screen?

I was disappointed with the highly editorial flavor of Charles Small's "Diagrammatic programming" (*EDN*, January 6, 1994, pg 60). I suspect that this article will generate much dialogue, mostly in defense of text-based programming. When Small uses words such as "endless," "bottomless," and "vainly" to describe text-based programming or statements such as "diagrammatic programming can make easy what were once difficult software tasks," my snake-oil detector goes off.

Whenever the latest idea comes into vogue, people make great claims about it, as well as how it will change the world. Sometimes, the idea *was* great, but its implementation was bad, and sometimes, the idea proves to be not so great after all. In either case, often the idea—no matter how great—simply couldn't live up to the glorious claims made by people who are honestly trying to move the world forward. What usually happens is that their good intentions backfire, and what could have been innovative is dropped like a hot potato (only to be "rediscovered" 10 or 20 years later).

I have decided to keep my mind open to diagrammatic programming, in spite of this highly opinionated article.

*Don Ausherman*
*Wichita, KS*

## Techie Nostradamus envisions future

Currently, you may feel confined by the legacy of the 8086, but it looks as if that old design will be the leader in the advance to virtual-memory processors built right on the DRAM (dynamic RAM). The ARM6 may be better in some ways, but the venerable 486 is not far from perfect for the job.

One advantage of a VMP (virtual-memory processor) is its low pin count. A VMP needs no address lines and uses most of the pins for data. The elimination of the address bus comes from having on-chip main memory—just as the elimination of separate memory paths for the Harvard architecture came from having separate on-chip caches. VMPs simply stream data to and from disk and other I/O in NT-like packet messages.

With an integrated main memory, the DRAM row-data latches, which would normally hold bits for static-column-mode access, are used as cache and as expanded register file. This avoids the function duplication that is characteristic of today's systems.

If a VMP were built on a 4-Mbyte DRAM, the chip may not be much bigger because the indigenous DRAM row-data latch could provide most of the processor's cache and register file. An additional 256 bytes of register file would come from each row latch that is added to the DRAM. Testing proves that a very small cache achieves most of the available benefit.

One row latch must serve as cache for instructions. An additional row should serve global data, and one should serve the stack. The 486 fits because one row latch can be devoted to each of the CS, DS, ES, and SS memory segments. You can achieve even more speed if the stack segment has two row latches so that local variables are available even at row boundaries (the BP in the 486 mates well to this need). Maintain write-back coherency by not permitting two row latches to open on the same row.

Using row latches as the register file of the new 486-style processors works because, in practice, most code works primarily on variables that are near the top of the stack. Since these row latches are part of the register file, the new processor will outperform register-rich processors. The register file will be an associative cache composed of the stack-row latches.

*Jack Jenkins*
*IST Corp*
*Lansing, MI*

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| DC 1 Year Accuracy | **0.0035%** | 0.0030% |
| AC 1 Year Accuracy | **0.06%** | 0.08% |
| AC Bandwidth | **3 Hz to 300 kHz** | 20 Hz to 100 kHz |
| Interface | **HP-IB & RS-232** | GP-IB |
| Programming Languages | **Fluke 8840A/42A SCPI HP 3478A** | Fluke 8840A/42A |
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| Internal Storage | **512 readings** | None |
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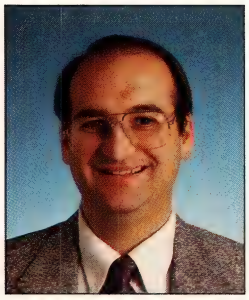
CIRCLE NO. 39

# Find your advantage



In case you hadn't noticed, there's a technological explosion taking place. This explosion has the force to remake the face of every market touched by the electronics industry. Here are just a few examples of the massive changes taking place:

☛ Logic vendors are curtailing the 20-year reign of standard logic by converting production to PLDs and FPGAs. Xilinx and AMD (which bought MMI) are the old-line product vendors here. Standard-logic vendor Texas Instruments has entered the field and Motorola is expected shortly. The conversion allows semiconductor vendors to get more revenue from their fabs and you get more capability, more compact designs, faster design turns, and lower system costs. You also have to learn how to use these parts and you have to buy the tools that allow you to work with programmable logic.

☛ The μP and μC vendors are proliferating processor families like mad. At the low end, Motorola seems determined to create not just a processor but an entire processor family for any need starting with the 68HC05K series (with parts that sell for less than a buck apiece) and ranging up through the 'HC08, 'HC11, 'HC16, and 'HC32. Even the venerable 68000—once the company's high-end, flagship 32-bit processor—now makes an effective, low-cost controller. At the same time, Philips seems determined to drive the 8051 architecture into as many applications as possible. Just look at the sub-$1 8XC750 for proof. (Be sure to enter the Philips Dream Machine Design Contest after you look at the 8XC750. You could win a new Camaro. See the April 14 issue of EDN for details.)

☛ At the high end of processor technology, things are busier than they've been for quite a while. Apple, IBM, and Motorola are trying to establish a 32-bit beachhead with the PowerPC. Intel is fighting back with clock-tripled '486s and proliferating Pentiums. Intel's competitors in the x86 market such as Cyrix, IBM, and TI are making sure you have plenty of alternatives in that market. There are an increasing number of versions of the Sparc and Mips processors and Digital Equipment Corp currently stands at the performance summit with its Alpha μP.

☛ Memory choices are at their widest ever. High-speed DRAMs from the Rambus partners (Fujitsu, NEC, and Toshiba) and cached DRAMs from Ramtron (the EDRAM) and Mitsubishi (the CDRAM) promise to smash the decades-long memory-bandwidth bottleneck. Intel has been working very hard to make Flash memories part of your future and Intel's competitors in the Flash arena such as AMD, AT&T, and Atmel also hope you learn to love Flash.

☛ Technology is moving nicely in the analog world too. For example, just as video is about to explode with all manners of interactive products and services, the big analog vendors such as Analog Devices, Burr-Brown, Comlinear, Elantec, Harris, Linear Technology, Maxim, and National Semiconductor are ready with the necessary video op amps and high-speed converters.

You must master some or all of these technologies to stay ahead in today's electronics industry. One thing all these technologies have in common is that they've all appeared in EDN. Our technical editors are engineers who understand the difficulties of design because they've all experienced design problems first hand. That's why they can write articles that fit your needs perfectly. So, to find your advantage, gaze deeply into the explosion including the technologies listed above; and continue to read EDN if you want to run twice as fast as you possibly can. EDN is dedicated to your success.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Steven H. Leibson

**Steven H Leibson**
**Editor-in-Chief**

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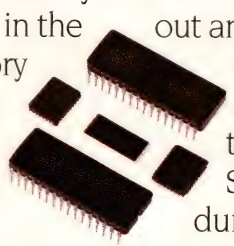

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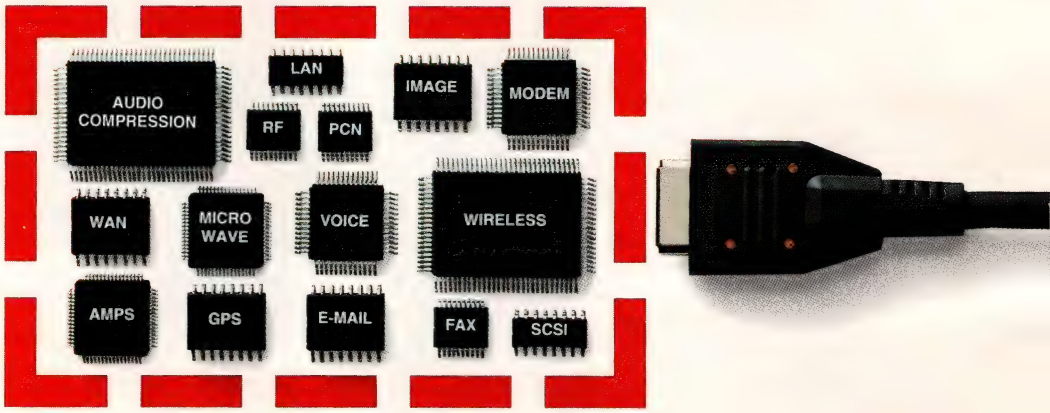


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CIRCLE NO. 48

WIRELESS EDA TOOLS

# EDA tools help fine-tune system design

DOUG CONNER, Technical Editor

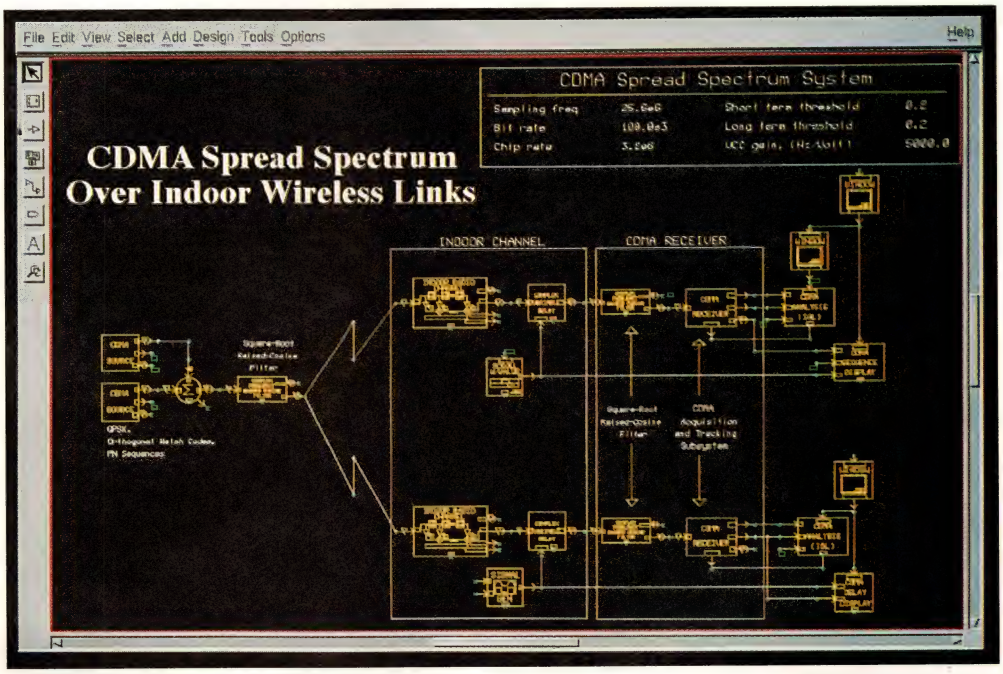
**By performing design iterations in software, EDA tools for wireless designs help you zero in on the right system design.**

Wireless systems have some of the toughest requirements in the electronics industry. Operating in an environment that may have atmospheric and electronic disturbances, wireless systems are often portable, necessitating compact size, low weight, and low power consumption to stretch battery endurance. DSP is fast becoming a standard feature on wireless systems too, adding computing power to the system requirements. Careful system design is necessary to create wireless designs that live up to their potential.

Electronic-design-automation (EDA) tools can help you develop wireless systems by letting you assemble the system in software before you actually build the hardware. Using a software simulation lets you perform a detailed analysis of the system's performance before you build it. Although analysis itself doesn't make a better system, it gives you a better understanding of the system so that you can determine what, if anything, needs improvement.

EDA tools at their most basic level can automate functions you once performed manually, such as schematic capture and physical layout. Although EDA tools that automate these tasks are more efficient than using manual design, the tools' greatest benefit is that they allow you to start a system design at a high level and work with a top-down design methodology. You model the system at its highest level and then simulate how the system behaves to inputs. Your system specification should guide you as to what to simulate and the level of detail you require.

The sooner you can get a handle on how your system will perform, the sooner you can get on a predictable development path.




**The Signal Processing Worksystem (SPW) from Comdisco Systems lets you model and simulate wireless communication systems, such as this code-division multiple-access design.**

## WIRELESS EDA TOOLS

Of course, no design that advances the state of the art is completely predictable. You can't even be sure it's possible until a system is operating. Simulation, however, can go a long way toward verifying that a system will work. Furthermore, until you determine that your system design is satisfactory, designing details will be a waste of time.

**Design with fewer iterations**

The time you spend developing a system-level simulation is time taken away from other design tasks. In addition, EDA tools cost money, and training takes time away from productive design work. Even after training, it takes time to become really proficient with the tools. How do you know all this time and money is well-spent?

One way is to look at historical results within your company. If it takes several iterations of a design to get the final product right, then you can improve your current product-development methodology. Even removing one iteration could save time and money. A top-down design methodology could potentially save one or more iterations in developing a design.

If your current design methodology doesn't result in multiple iterations to reach your desired product, your method may be satisfactory. However, you should still consider the impact system simulation may have on your product. For example, you may design a better product with simulation because it allows you to experiment with design changes to see how they affect the system's overall performance. One of the major benefits of simulation is that it lets you quickly test many design changes.

**Complex considerations**

Almost any electronic design can benefit from system simulation, and wireless systems have a variety of complicating considerations that make system simulation particularly helpful. For example, many wireless systems, especially those for communication, use complex modulating schemes to transmit as much data as possible through a given portion of the electromagnetic spectrum. You cannot use simple calculations to approximate the performance of these complex modulation schemes. Furthermore, the wireless environment is a demanding one in which transmissions may be subject to interfering signals, reflections, weather-related effects, and other disturbances that make analyzing performance difficult.

Another aspect of wireless design is a trend toward the increasing use of DSP, which adds another variable to the design process. A typical DSP design requires you to consider cost and performance tradeoffs on the level of DSP vs analog signal processing.

DSP can make the performance of a system less sensitive to manufacturing variations. The performance of an analog design, however, varies from unit to unit, primarily due to component vari-

### WIRELESS EDA TOOLS

| Manufacturer | Product | Price | Description |
|---|---|---|---|
| **Cadis**<br>**Circle No. 323** | Cossap | $30,000 | Designs and simulates DSP systems; generates C code for programmable DSPs and for general-purpose μPs; generates VHDL for simulation and synthesis; includes telecomm libraries |
| **Comdisco Systems**<br>**Circle No. 324** | SPW | $25,000 | Describes DSP systems with block-level diagrams and works them down into digital implementations; designs and simulates fixed and floating-point designs and single-processing and multiprocessing appplications; generates C, assembly, and VHDL code; offers a library of communication elements for wireless system design |
| **Elanix**<br>**Circle No. 325** | SystemView | $985 | Windows-based dynamic system simulator for signal-processing and communication systems, including analog, digital, and mixed-mode systems; works with multirate systems and systems with mixed discrete and continuous time elements; also appropriate for control systems and mathematical modeling |
| **HP-EEsof**<br>**Circle No. 326** | OmniSys | $26,000 | System simulator for evaluating topologies of wireless systems; analyzes complex waveforms in systems based on arbitrary topologies and modulation schemes; typical applications include digital and analog cellular radio, global positioning satellites, collision-avoidance systems, wireless LANs, terrestrial-microwave and satellite communications, radio, television, and radar |
| **Hyperception**<br>**Circle No. 327** | Hypersignal for Windows Block Diagram | $1995 | Block-diagram simulator especially for DSP designs; offers an optional advanced transmission library ($1495) that provides a set of design and analysis blocks for radio, wire-line, and fiber-optic transmission systems |
| **Mentor Graphics**<br>**Circle No. 328** | DSP Station | $33,000 | Includes design, simulation, and analysis tools for DSP development; offers an optional telecomm simulation library with more than 300 complex functions for telecomm and VHDL generation (primarily for simulation); offers implementation options, including code generation for programmable DSPs and architectural-synthesis tools for ASIC and IC implementation |
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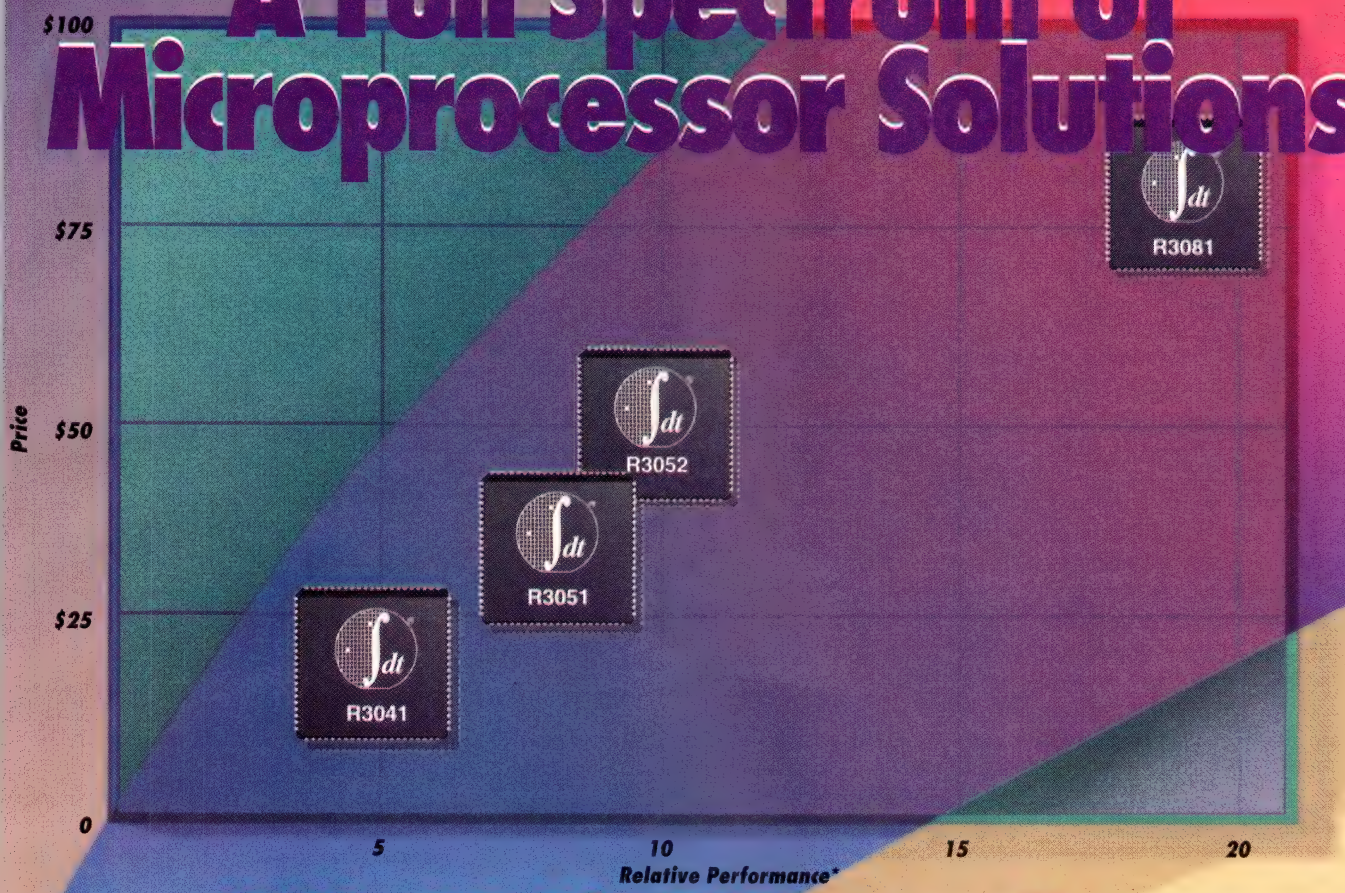


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## WIRELESS EDA TOOLS

ations in resistors, inductors, and capacitors (although a properly designed analog product can accommodate analog-component variations and still meet performance specifications). Digital systems, on the other hand, perform identically on all units. In addition, in many cases, especially at the lower-frequency portions of wireless systems, DSP provides performance superior to that of analog and at a lower cost.

Portions of wireless systems will remain analog for a long time to come. For example, the RF portion is currently always analog, and DSP techinques are just starting to become viable for some IF applications. You can best find the proper mix of analog signal processing and DSP by simulating the system as a whole to make sure the performance is up to the specification. You can then evaluate which approach provides the lowest total system cost.

### Experiment with tradeoffs

Creating a system simulation can be relatively quick if you have a library of models that covers the system components you need; acquiring or developing new models, however, takes time. Once you develop a simulation, it becomes relatively easy to make small design changes and run the many system tradeoffs necessary to analyze and settle on a design.

Once you settle on a design, you can move on to designing the details of the system. One of the great benefits of simulating and iterating a design until the simulation indicates that a system will meet your requirements is predictability. If you start with a system simulation and develop a top-level design that works, then you have a predictable design process as you work to change each block in the simulation into a detailed circuit performing the functions required.

Choosing the proper system simulator for wireless designs means finding one that fits your design process. One of the most important considerations in choosing a simulator is the product's model library.

### The importance of models

Models are the currency for simulators: Without models, a simulator is useless. When you shop for a simulator, spend plenty of time examining the model libraries to make sure the model goes into the level of detail you require. For most wireless work, you need a library of models specifically dedicated to telecomm design.

The model library needs to include models not only for system components, such as amplifiers and mixers, but also for modulation schemes, atmospheric degradation, and other parameters. If you cannot obtain the models you need in a library, you can obtain them from other sources. For example, the simulator vendor may develop models for a fee, and manufacturers of wireless-system components sometimes develop models. Alternatively, you can develop the models yourself.

You also need to evaluate how the simulator works with the rest of your design tools as you go from a top-level system design down to a detailed design. If you are doing only the top-level system design, and someone else or another company is designing the modules that go into the system, then you don't necessarily need the simulator to work with lower-level design tools. However, if you are designing the modules or function blocks that comprise the system, you might want to be able to simulate each block and drop them back into the system simulation to see if the block still performs as expected.

As your design progresses from a block-level system design into a detailed design, you need to decide what level of fidelity you need from the simulator in representing the real system. High-level system simulators shouldn't have difficulty representing both digital and analog portions of wireless systems. As you move down into detailed design, you may require more sophisticated mixed analog-digital simulation.

Systems with DSP blocks require special consideration. For example, you may simulate your system at the top level with a floating-point representation. As you work out the detail design, you may actually be using fixed-point processing for higher speed and lower cost. The floating-point representation now needs to change to represent the quantization effects of the fixed-point computations. The ability to represent the actual resolution of the hardware is called "bit-true simulation."

You may place other requirements on a wireless-system simulator. It may take time to find a simulator, acquire or develop the models, and learn to use the tool effectively. In the long run, though, it should help you design the system you want with fewer iterations. EDN

*You can reach Technical Editor, Doug Conner at (805) 461-9669, fax (805) 461-9640.*

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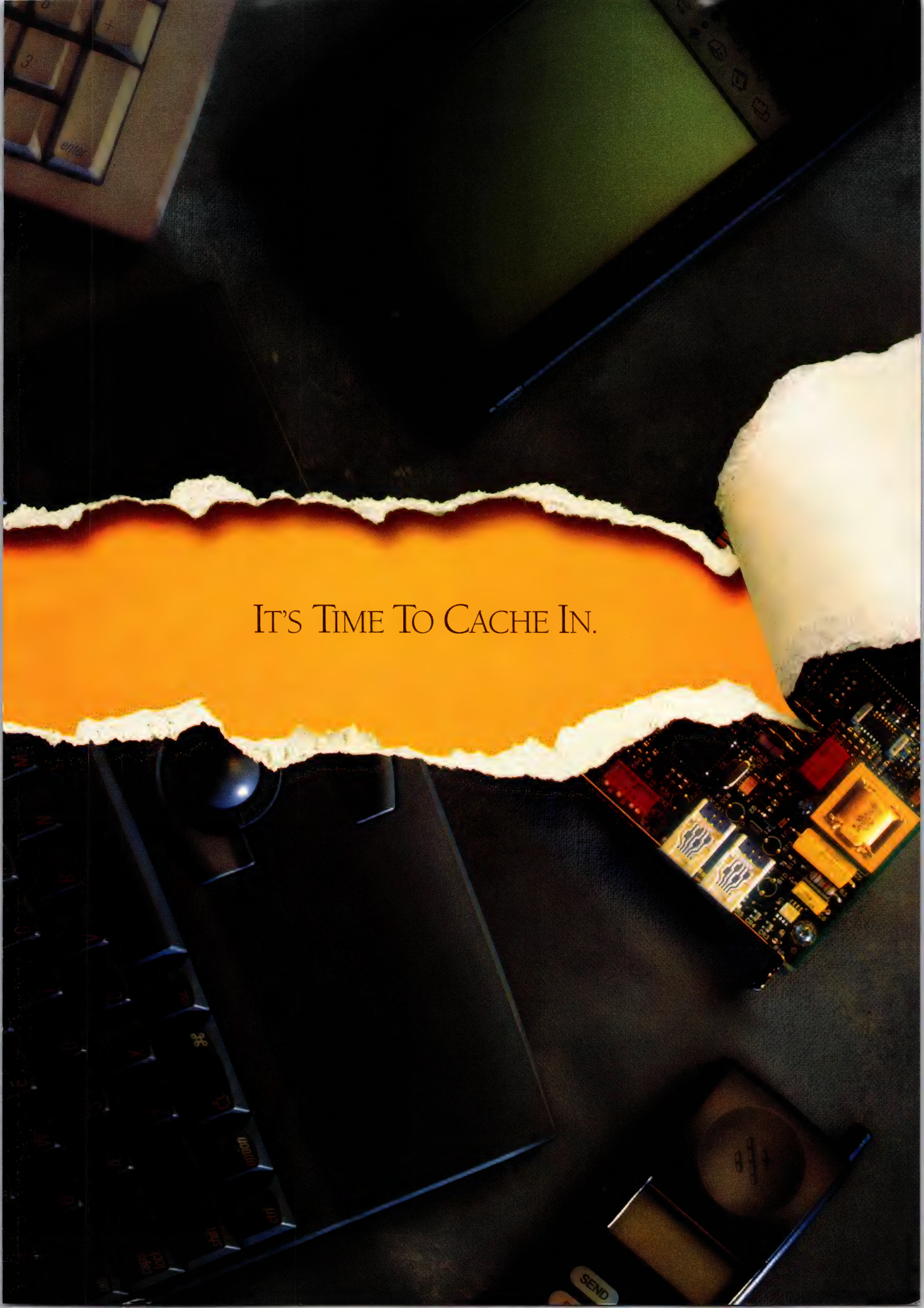
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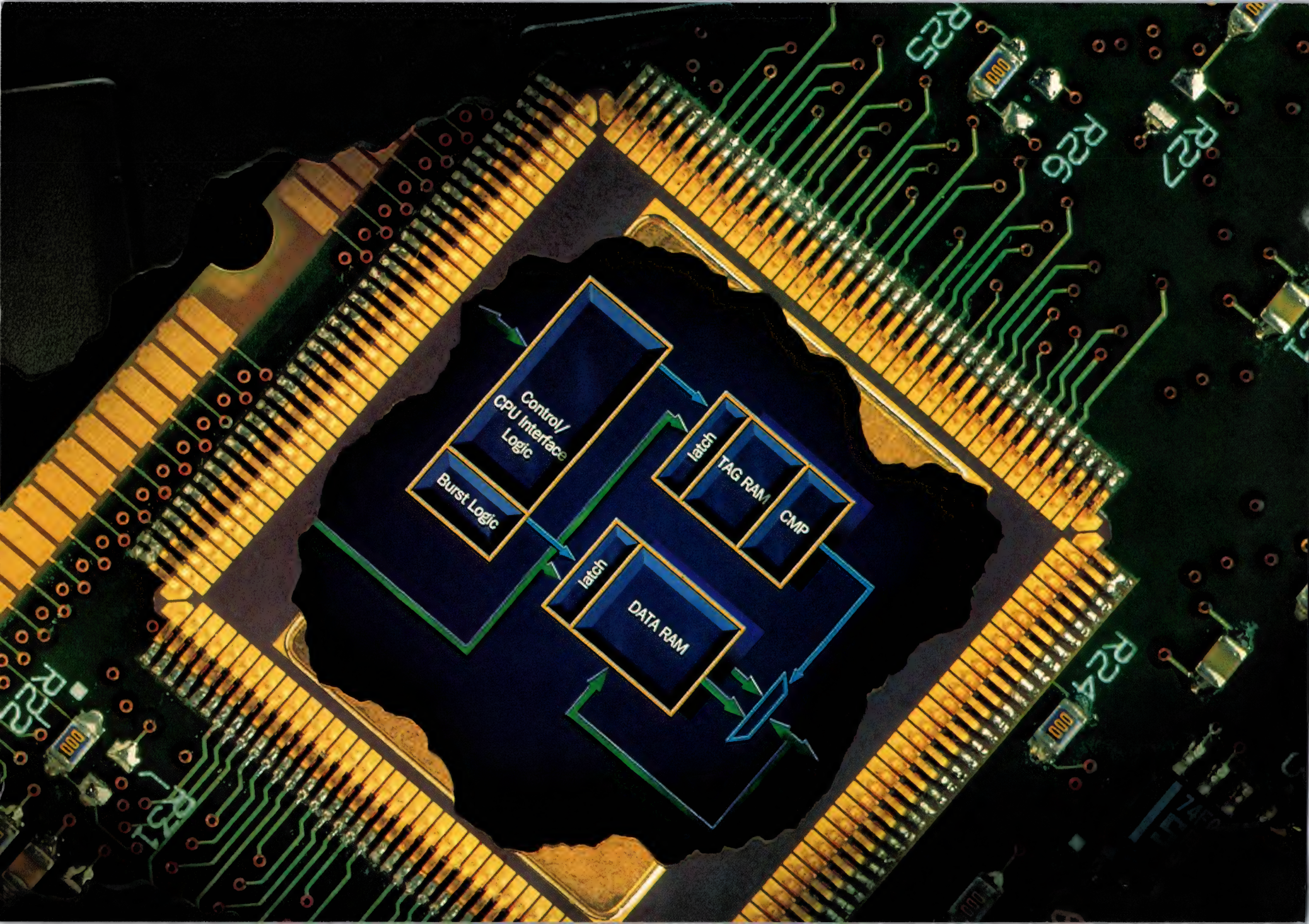
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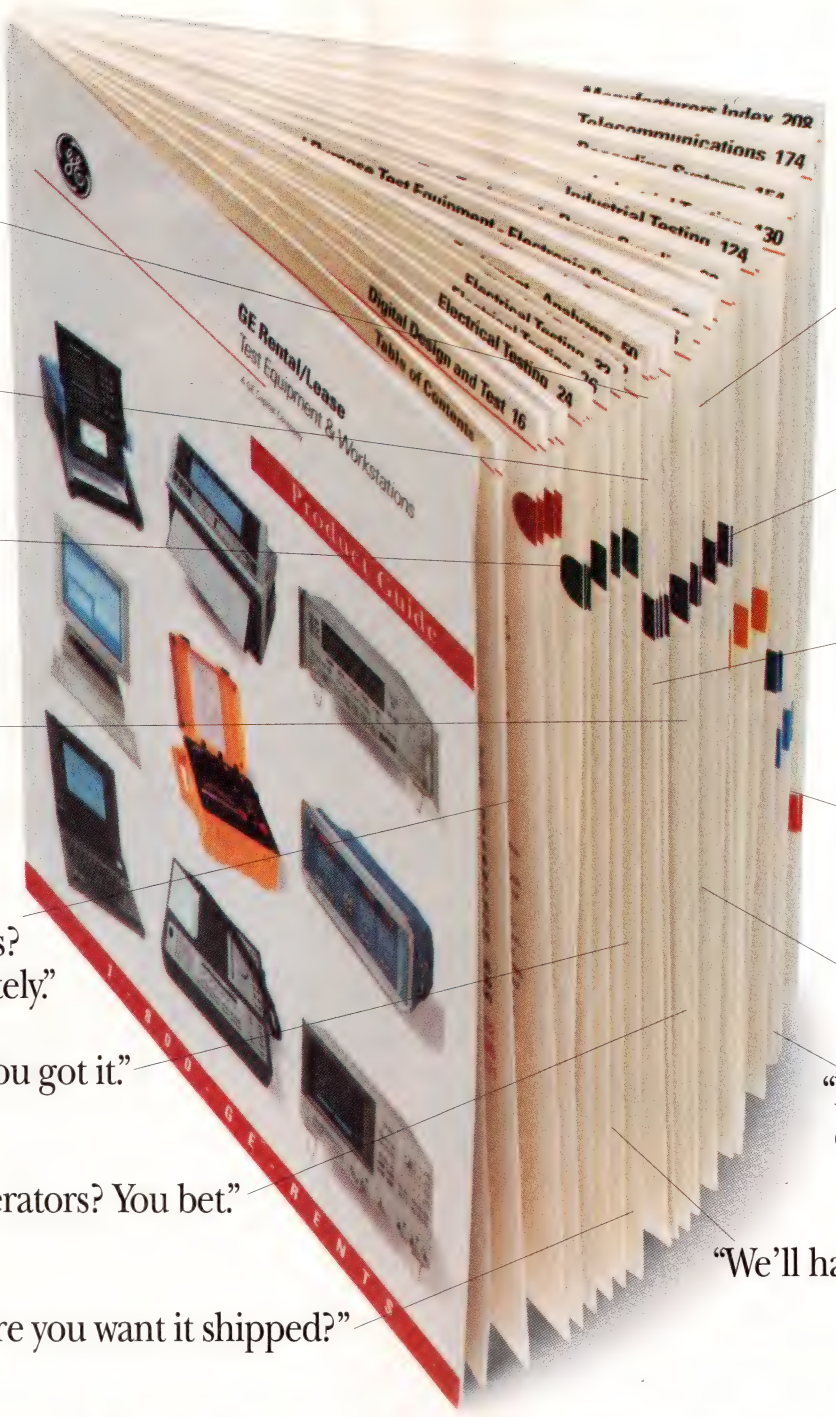


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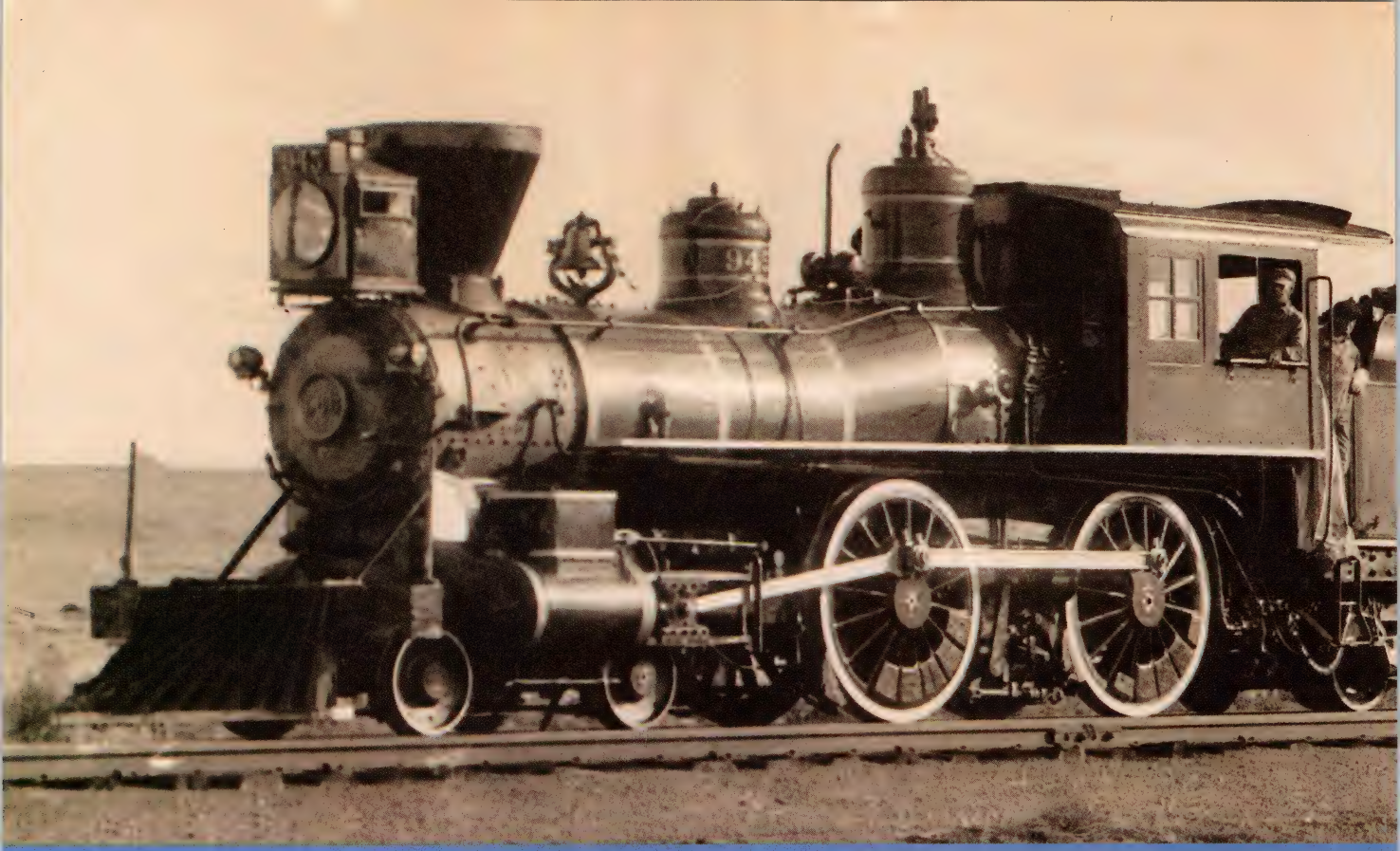

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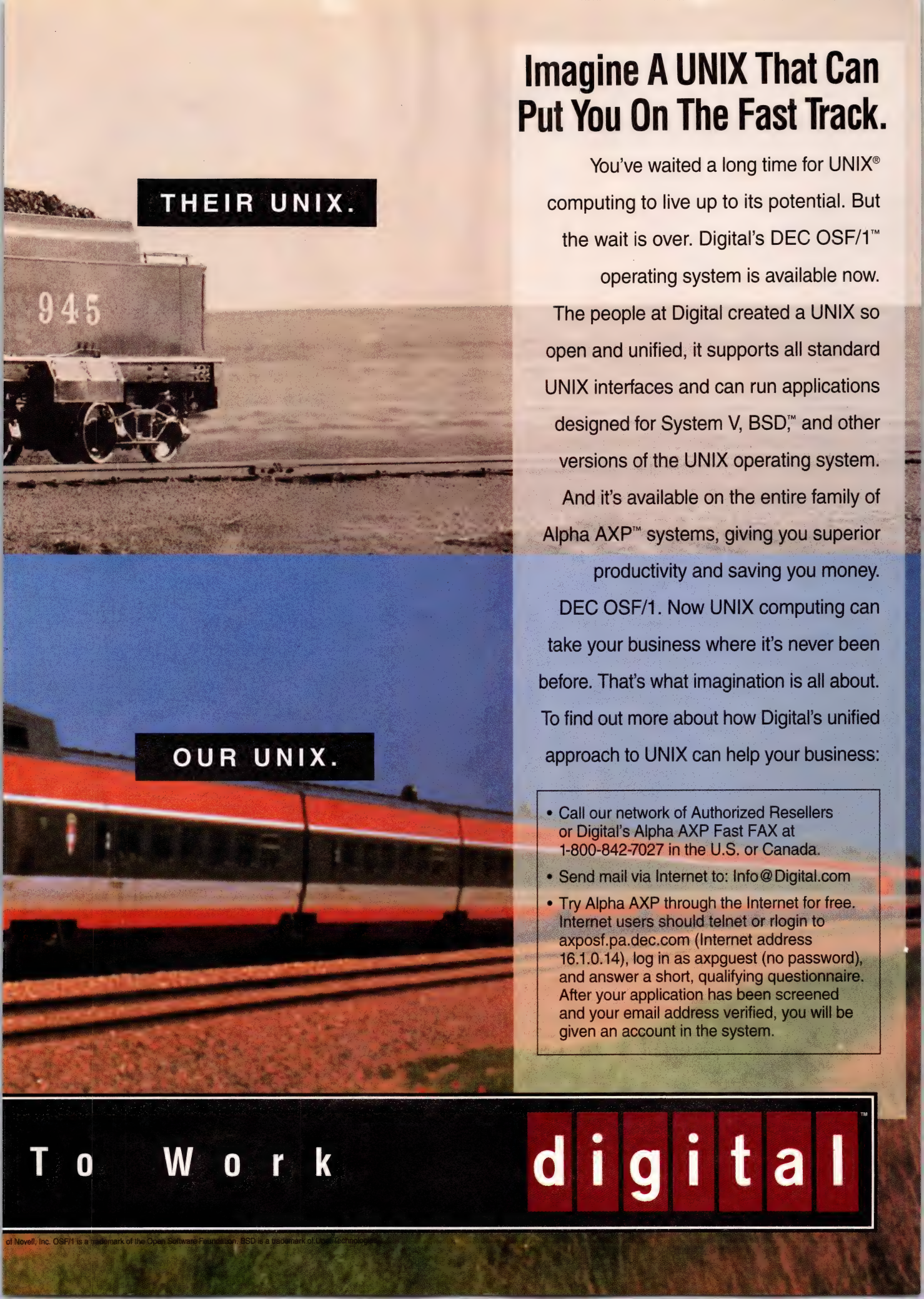


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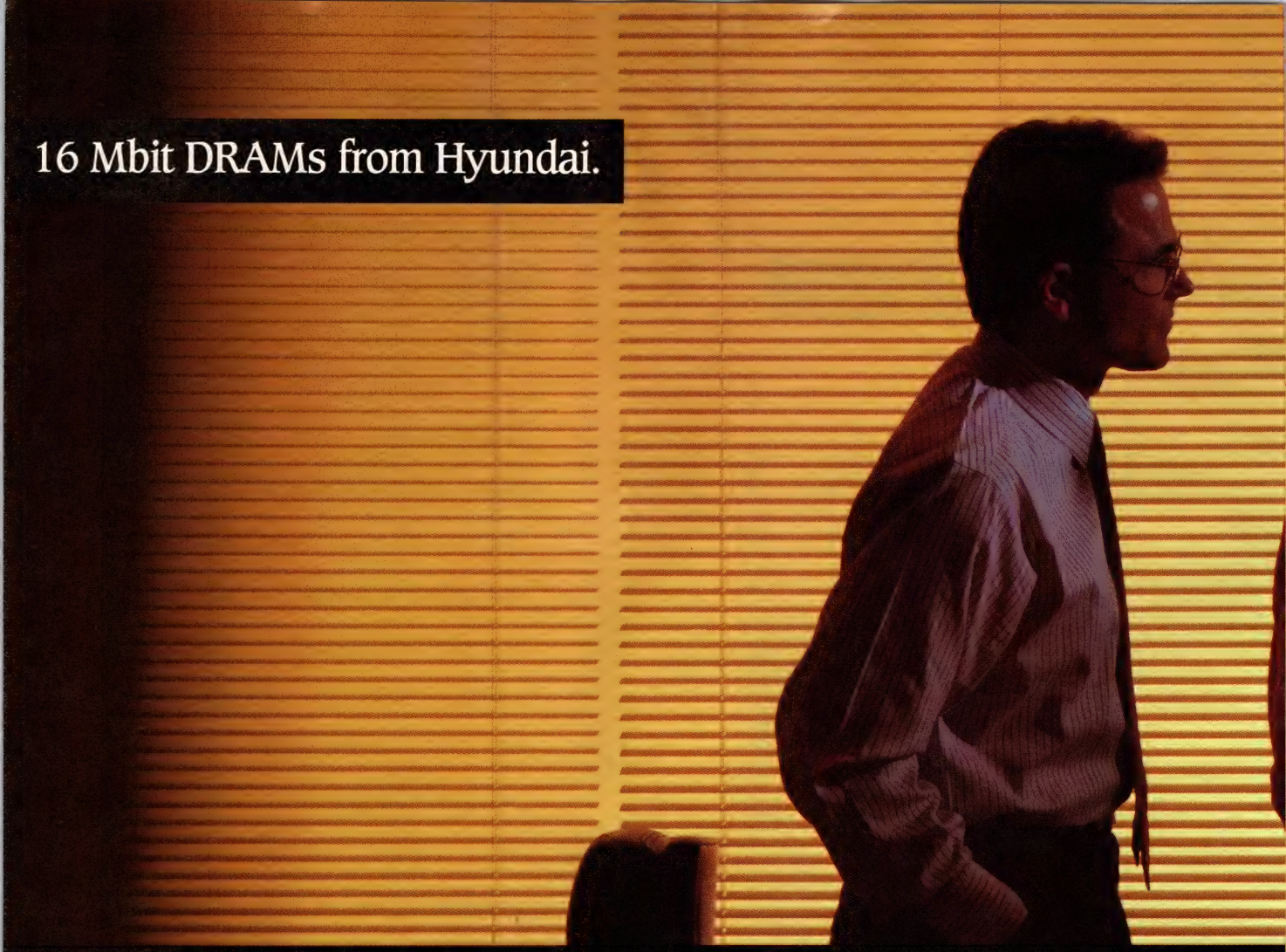
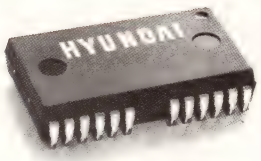


# Team Dy




Sourcing used to be simple. The buyer and the design engineer got together for a few minutes. And that was it.

No more!

Now, virtually all of the make or break purchases for DRAMs and other major ICs in companies with over $10M in sales* are the result of a cross-functional team dynamic. And remember, no company has a bigger commitment to team dynamics than Hyundai.

Hyundai knows the engineer needs better performance from the technology. Production must have qualified, readily obtainable parts. Purchasing has to get the best possible price and delivery. And management must build a long term strategic partnership with suppliers to obtain a superior competitive advantage.

Our new 16 Mbit dynamic RAMs are one more example of our dedication to the needs of the new team dynamic. We're committed to your success and the success of your cross-functional buying team through Hyundai's commitment to quality, reliability, manufacturing capability and value added pricing.

**Your Hyundai DRAM Source Guide**

| Size | Part Number | Speed ns | Refresh Cycles/ms | Production |
|---|---|---|---|---|
| 16M x 1 | HY5116100 | 60/70/80 | 4096/64 | now |
| | HY5117100 | | 2048/32 | |
| 4M x 4 | HY5116400 | 60/70/80 | 4096/64 | now |
| | HY5116410 | | 4096/64, WPB | |
| | HY5117400 | | 2048/32 | |
| | HY5117410 | | 2048/32, WPB | |
| 2M x 8 | HY5116800 | 70/80 | 4096/64 | Q4 '94 |
| | HY5116810 | | 4096/64, WPB | |
| | HY5117800 | | 2048/32 | |
| | HY5117810 | | 2048/32, WPB | |
| 1M x 16 | HY5116160 | 70/80 | 2$\overline{CAS}$, 4096/64 | Q4'94 |
| | HY5116260 | | 2$\overline{CAS}$, 4096/64, WPB | |
| | HY5118160 | | 2$\overline{CAS}$, 1024/16 | |
| | HY5118260 | | 2$\overline{CAS}$, 1024/16, WPB | |

All available in standard and low power versions.
Packages include SOJ, TSOP II, reverse TSOP II.


**New 16 Mbit DRAMs, designed with team dynamics in mind.**

Evaluation samples of Hyundai DRAMs organized 16M x 1, 4M x 4 are available now. Coming soon are DRAMs organized 1M x 16 and 2M x 8. And many will operate off of a 3 volt source too.

Hyundai's new DRAMs feature speeds of 60, 70, or 80 ns. Immediately available, the HY5116100 and HY5117100 are organized 16M x 1 and provide 4096 refresh cycles per 64 ms and 2048 refresh cycles per 32 ms, respectively. New 4M x 4 parts include the HY5116400, with 4096 refresh cycles per 64 ms, the HY5116410 with write-per-bit capability, and the HY5117400 and write-per-bit capable HY5117410 offering 2048 refresh cycles per 32 ms.

All parts are available in standard and low power versions, dissipating 495 mW operating at 60 ns, 440 mW at 70 ns, and 385 mW at 80 ns. Other features include operation from a single 5V ±10% power supply, TTL compatible inputs and outputs, fast page mode operating, multi-bit test capability, read-modify-write capability, and CAS-before-RAS, RAS-only, as well as hidden refresh. Packages include standard 24/28 pin plastic, TSOP II, and reverse TSOP II. TSOP will be available soon.

These new parts are products of Hyundai's 0.55 micron CMOS process, at one of the most advanced electronics manufacturing plants in the world. So if purchase of 16 Mbit DRAMs is on your agenda, and you don't want to get caught short the way some did on 4 Mbit, start the team dynamics now.

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INDUSTRIAL BUSES

# Network vendors agonize over fieldbus standard

BRIAN KERRIDGE, Technical Editor

**The process-control industry is teasing out a global standard for a digital-communications bus from an assortment of proprietary and national standards. Frustrated by the slow progress, however, vendors and users are looking for bus systems they can adopt today.**

Mention "fieldbus," and the entire process-control and factory-automation communities heave a mighty sigh—not of relief, but of sheer irritation, impatience, and confusion. In an effort to establish an international fieldbus standard and with a workable standard probably more than five years away, market forces have compelled two quasistandard bodies to publish, promote, and support their complete—but different—specifications for a fieldbus. These bodies, with the unlikely titles of Interoperable Systems Project (ISP) and World Factory Implementation Protocol (WorldFIP), have each sworn allegiance to the official developing standard and to converging their specifications with whatever the standard finally becomes.

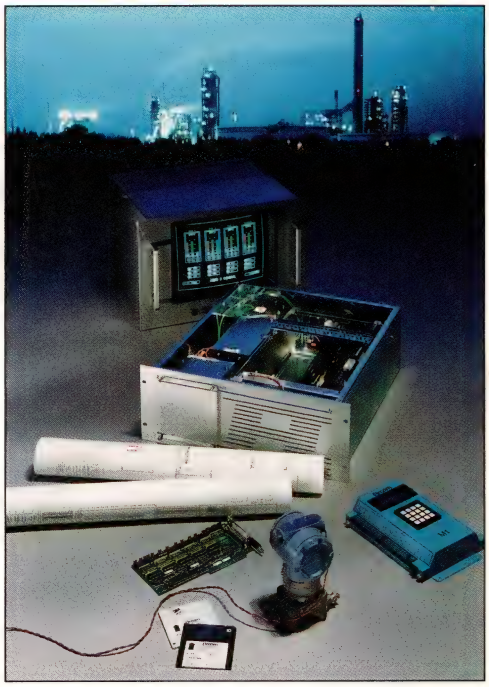
Against this confusing and uncertain background, designers of process-control and factory-automation products must decide how to proceed. Falling into line with ISP or WorldFIP means designing on a foundation of slowly shifting sand. Some level of early obsolescence seems unavoidable.

Certainly for the short term, companies that want their products ultimately to conform face a dichotomy: Which army will march the shortest route to the standard? Each side is assembling an armory of silicon and design tools, field trials are in progress, and the battle is about to commence. And, by the way, shoot the first guy who says maintaining conformance means changing only a bit of software.

"Fieldbus" is a generic term describing a digital, bidirectional, multidrop, serial-bus, communications network to link isolated industrial field devices, such as sensors, actuators, and controllers. Overall, by installing low-cost computing power in each field device, fieldbus will replace centralized control by distributed-control networks. Fieldbus will also improve data integrity and introduce device control, calibration, and diagnostic functions. Other benefits, including lower installation and maintenance costs, result from substantially simpler plant cabling.

Considering the maturity of the process and automation industries, you might expect there to be at least some de facto standard digital network. In reality, however, nothing could be further from the truth: The most standard feature of today's industrial-control systems is still the 4- to 20-mA analog signal that has been in use for decades.

But don't imagine that the absence of a digital standard results from any lack of resolve on the part of officialdom. Since the mid-1980s, the Instrument Society of America (ISA) and the International Electrotechnical Commission (IEC) have made tremendous joint efforts to establish a unified fieldbus standard. But, despite their efforts and the volumes of draft documents in cir-



**Fieldbus introduces distributed-control networking to future process-control and factory-automation systems. The system significantly advances plant design and management in data integrity; device control, calibration, and diagnostics; and plant cabling.**

BBS Listings of ISP and WorldFIP ICs and support tools are available on *EDN*'s computer bulletin-board system. Phone (617) 558-4241 with modem settings 300/1200/2400 8,N,1. Access */freeware* IG and specify the *(r)ead* option followed by *(k)eyword* search for "TU417."

culation, ISA/IEC have so far published a specification (**Ref 1**) for only Layer One—the physical layer—of a fieldbus.

A multitude of problems, none of which is technology-based, has dogged ISA/IEC's drive for a complete standard. The main difficulty is achieving consensus among the many heavyweight players in the process-control and factory-automation industries. These system suppliers have jealously protected an immense installed product base and substantial future interests. Equally, some suppliers—with hitherto-proprietary bus schemes—are slow to accept the concept of an "open" standard and the prospect of product interoperability.

Other reasons for the delay relate to the ambitious scope of the proposed standard. Although primarily for communicating between field elements in the process industry, the standard will also apply to plant automation in building, manufacturing, and transportation. The standard will specify all layers of an ISO/OSI 7-layer model for a communication protocol and will include an eighth user layer to ensure full product interoperability.

Interoperability, a key fieldbus objective, permits straightforward substitution of bus devices from different manufacturers without affecting overall system performance. Toward that end, all bus devices will contain a software-function block or blocks and a software-device description appropriate to the device. For example, a sensor will contain an "analog-input" function block, and an actuator will contain an "analog-output" block and maybe a "3-term-control" block. The device description differentiates between similar types of devices, such as high- and low-temperature-range sensors. With function blocks, device descriptions, and "set-point" data from hosts, a sensor and an actuator will work together over the fieldbus, forming a separate control system.

### NEW BOOK FOCUSES ON FIELDBUS

On June 1, UK-based GGH Marketing Communications, consultant to the field-communications and control-instrumentation industries, will publish *The Fieldbus Book*. The book contains a directory of fieldbus products, including chips, development systems, networking products, field devices, and controllers. To obtain a copy, contact Geoff Hodgkinson, GGH Marketing Communications, Titchfield, UK. 44 (329) 846166.

**ISP and WorldFIP set up shop**

Both ISP and WorldFIP have set up organizations to promote their versions of fieldbus. These organizations offer a wide range of services, including publishing specifications, newsletters, and catalogs; offering sources of silicon and design tools; providing seminars, training programs, and field-trial support; and coordinating product-compliance testing. Most of these services support organization member companies. What a company pays for membership depends on its size and the level of support it requires. ISP's annual charge ranges from $1000 to $75,000 for companies with sales of more than $100 million. WorldFIP's annual charge, which is double in the first year, ranges from $1000 to $12,000 for companies with 1000 or more employees.

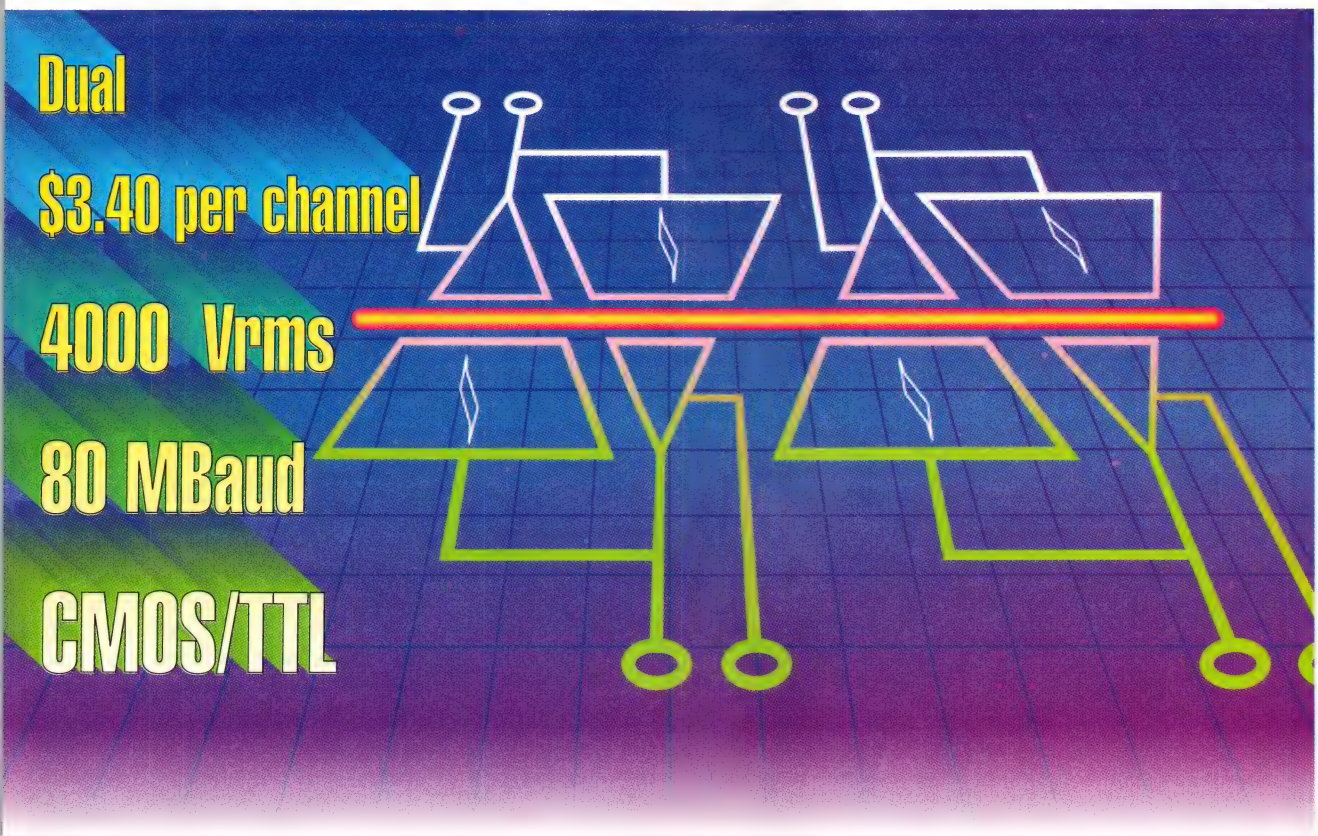
ISP's principal subscribers include Fisher-Rosemount, Foxboro, Siemens, and Yokogawa. Behind WorldFIP are Allen-Bradley, Honeywell, Square D, and a strong contingent of French companies, including Cegelec, Electricité de France, Elf, and Telemecanique. WorldFIP's French influence comes from an earlier French National Standard, NFC 46-600, also known as FIP, from which WorldFIP developed. By comparison, ISP emerged largely from a German National Standard, DIN STD 19245, also known as Process Field Bus (Profibus).

### TABLE 1—FIELDBUS VERSIONS

| | ISA/IEC | ISP | WorldFIP | LonWorks | HART |
|---|---|---|---|---|---|
| **Media** | Twisted pair | Twisted pair | Twisted pair | Twisted pair, power line, wireless | Twisted pair |
| **Data rate** | 31.25 kbps (H1), 1 or 2.5 Mbps (H2) | 31.25 kbps (H1), 1 or 2.5 Mbps (H2) | 31.25 kbps (H1), 1 or 2.5 Mbps (H2) | 38 or 78 kbps, 1.25 Mbps | 1200 bps |
| **Line length (m)** | 1900 (H1), 750 (H2) | 1900 (H1), 750 (H2) | 1900 (H1), 750 (H2) | 1200 (38 kbps), 2000 (78 kbps) 500 (1.25 Mbps) | 1500 |
| **Maximum no. of nodes** | 256 | 32/segment, 125/region, 64 regions | 256 | 127/subnet 32,385/domain | 15 |
| **Data-link layer** | No specification | Token-passing, centralized | Centralized | Carrier-sense multiple-access | Dual-master centralized |
| **User layer** | No specification | Implemented | Implemented | Not implemented | Implemented |
| **DC power on bus** | Yes | Yes | Yes | Planned | Yes |

NEW

# Isolated Bi-Directional Digital Coupler

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## INDUSTRIAL BUSES

Both FIP and Profibus remain alive and well, although fieldbus purists despise the inability of these buses to be "intrinsically safe." Intrinsic safety, an important option for any future fieldbus system, refers to the power level a device can transmit along the bus—a significant factor when a device is processing flammable material, for example. This safety limit also accommodates another fieldbus option that requires bus cables to carry dc power to field devices. Both FIP and Profibus fail to conform to current intrinsic-safety limits because they are based on high-level signaling and because they require 4-wire cables compared with a single twisted pair for the fieldbus.

If you're not already confused, take a look at **Fig 1**, which shows the origins of the three main fieldbuses. However, **Table 1**, a comparison of the salient features of the main fieldbuses and their alternatives, might allay some of the confusion.

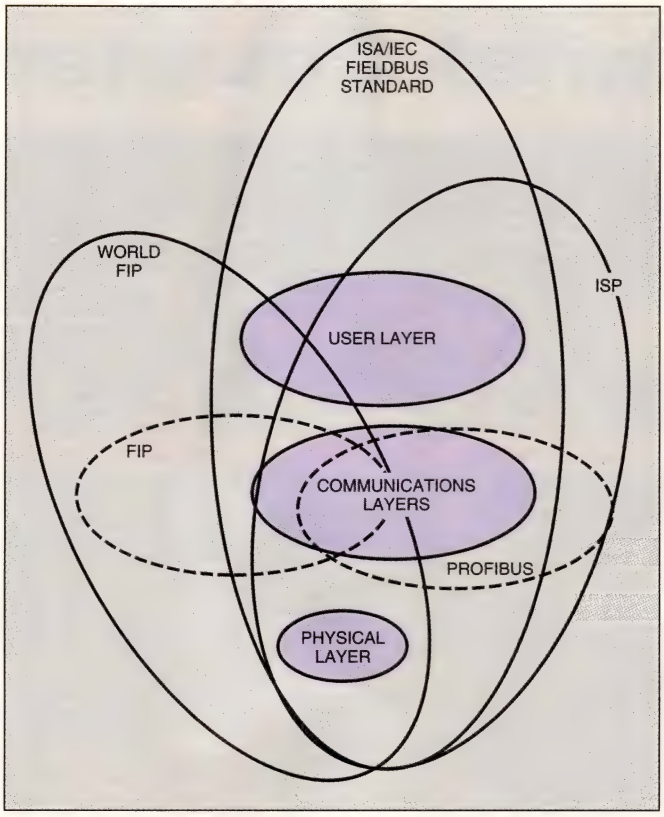


**Fig 1—The complex origins of fieldbus offer significiant obstacles to evolving a single global standard. Ultimately, if all goes according to plan, the three large ovals representing ISA/IEC, ISP, and WorldFIP should increasingly overlap and unite.**

The first silicon that supports ISP or WorldFIP comes in the form of device-communication controllers. Generally, these controllers handle all physical-layer functions and, to various degrees, functions in the data-link layer. In these products, 8-bit register interfaces allow direct connection via an Intel- or Motorola-type bus to a device's host processor.

Among the companies offering such controllers are Fuji Electric and Yokogawa. Both companies' controllers support ISP protocols. For the lower 31.25-kbps data rate (H1), Fuji and Yokogawa offer the Frontier-1 and Find-1 controllers, respectively. For the higher, 1- or 2.5-Mbps data rates (H2), Yokogawa offers the Find-2 chip-set pair.

Another company, Shipstar Associates, claims that its Fchip-1 series of controllers supports both ISP and WorldFIP protocols at either high or low data rates. Fchip-1 uses Actel ASIC technology and later will use AMI ASICs when Shipstar begins manufacturing the devices in large volumes. Shipstar also offers a wide range of support tools.

You can also obtain WorldFIP controllers and a PC-based development kit ($15,000) directly from WorldFIP. Controllers include FullFIP2 from Cegelec and FIPC01/2/3 from Telemecanique.

If entering the main battle is not for you, there are other, more immediate and proven routes to a fieldbus. For example, Echelon's LonWorks control network and Rosemount's Highway Addressable Remote Transducer (HART) protocol represent viable alternatives.

Barry Haaser, Echelon's marketing director, shows scant concern that the company's LonWorks is not wedded to a global fieldbus standard. In fact, he believes it's unlikely that such a standard will ever emerge. If you look at the nature of the industry and its players and the history of FIP and Profibus, you see the same battle continuing and moving to the United States, says Haaser. He believes that it's unlikely that we'll see a clear-cut winner.

Haaser says the most obvious need is for a fieldbus that's available today and, more important, that the fieldbus that emerges is at the sensor-network level

## LOOKING AHEAD

Having hauled the fieldbus juggernaut thus far, the Instrument Society of America (ISA) and International Electrotechnical Commission (IEC) technocrats are likely to see the task through to completion. However, the form the SP50 specification will take and when it will arrive remain in doubt. Currently, Part 3, the data-link-layer service definition, and Part 4, the data-link-layer protocol section are at the public-review stage, which means both are likely to become part of the standard by year-end. Several drafts exist for other layers, including a physical-layer amendment to include a wireless medium, and a mammoth 1200-pg draft for a user-application layer. These drafts are at committee stage with no prospect of becoming standard in the short term.

From a designer's perspective, too much rhetoric surrounds the ISA/IEC, Interoperable Systems Project (ISP), and World Factory Implementation Protocol (WorldFIP) fieldbus subject. This rhetoric compounds the confusion already surrounding the complex origins of fieldbus. Unfortunately, this confusion encourages users and vendors to further delay a technology leap that promises a startling effect on the way we control our world.

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## INDUSTRIAL BUSES

of a control hierarchy. LonWorks finds most success at this level, which includes sensors, actuators, and distributed-I/O devices. The product range currently has over 700 users worldwide and includes around 100 OEM products. Echelon also offers a product-interoperability testing service.

LonWorks' major features include the wide range of media it supports (twisted pair, RS-485, fiber, power line, and wireless), its low cost ($10 to $20/node), and its size (2 $in^2$/node). LonWorks nodes use Neuron chip controllers from Motorola and Toshiba, and a comprehensive range of software-development and network-management tools are available.

Rosemount's HART protocol has the virtues of being fully developed, available, and well-supported. HART user groups boast an installed base of more than 500,000 units using this open-bus standard. Key to its appeal is the ability to carry a conventional 4- to 20-mA analog signal with digital data on one twisted pair. HART systems use a Bell 202 1200-bps FSK signal superimposed on the 4- to 20-mA signal. The FSK signal has no dc component, allowing the analog and digital data to coexist without interference. In practice, though, this system limits the digital message-transaction rate to three transactions/sec and multidrops/loop to 15 when you use HART in digital-only arrangements.

Mark Portlock, process-control products manager at Arcom Control Systems, says these limitations are not significant for many data-acquisition and maintenance systems and process-control systems with relatively long response times. He says HART particularly suits systems involving physical metering and control, in which temperature, pressure, or flow changes, for example, take seconds or longer. Factory-automation and process-control applications with response times requiring more than 10 message transactions/sec require the use of a high-speed fieldbus.

Portlock believes that 15 multidrops/loop is generous because, although the number of nodes in an overall system may exceed 15, sensors and actuators tend to be in clusters, which generally occupy different sites of a system. Thus, it's convenient to run separate loops to each cluster.

Portlock estimates a roughly 50:50 split between HART users that retain the 4- to 20-mA function and those wanting full digital multidrop operation. Users employing the mixed-signal arrangement use the digital path for data acquisition, control signals, and maintenance and calibration data—which is significant for ISO 9000-compliant systems.

Portlock reports virtually no pressure from users or potential clients to standardize on a designated fieldbus. However, Arcom is carefully tracking developments because the company sees higher speed and distributed-control performance as important for future systems business. Currently, though, Portlock says, the gray area surrounding the fieldbus makes it too early to predict the direction Arcom will take.

For more information on HART systems, the UK-based HART user's group publishes the "The HART Book," a directory of worldwide sources of HART-supported products. For further publications on HART systems, see **Refs 2** and **3**. EDN

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## References

1. "Fieldbus Standard for use in Industrial Control Systems, Part 2, physical layer specification and service definition," Instrument Society of America, SP50.02, 1992.

2. Bowden, Romilly, "HART Field Communications Protocol—A Technical Description," Rosemount, 1991.

3. "Developing Process Systems using HART," Arcom Control Systems.

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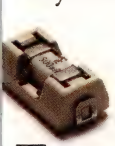

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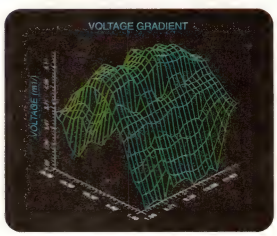
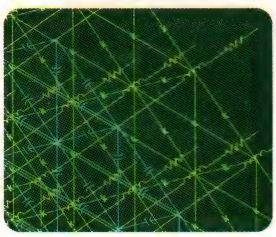
CIRCLE NO. 70

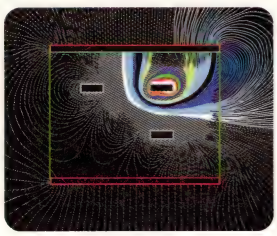
# HOW MANY AMPS DOES IT TAKE TO CHART A SURE COURSE TO A SOLID FIRST ARTICLE?

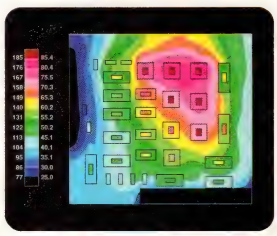

*3D voltage drop analysis.*



*3D matrix model improves CAE simulation.*



*2D, 3D electromagnetic analysis of interconnects.**



*Thermal analysis optimizes component placement.***

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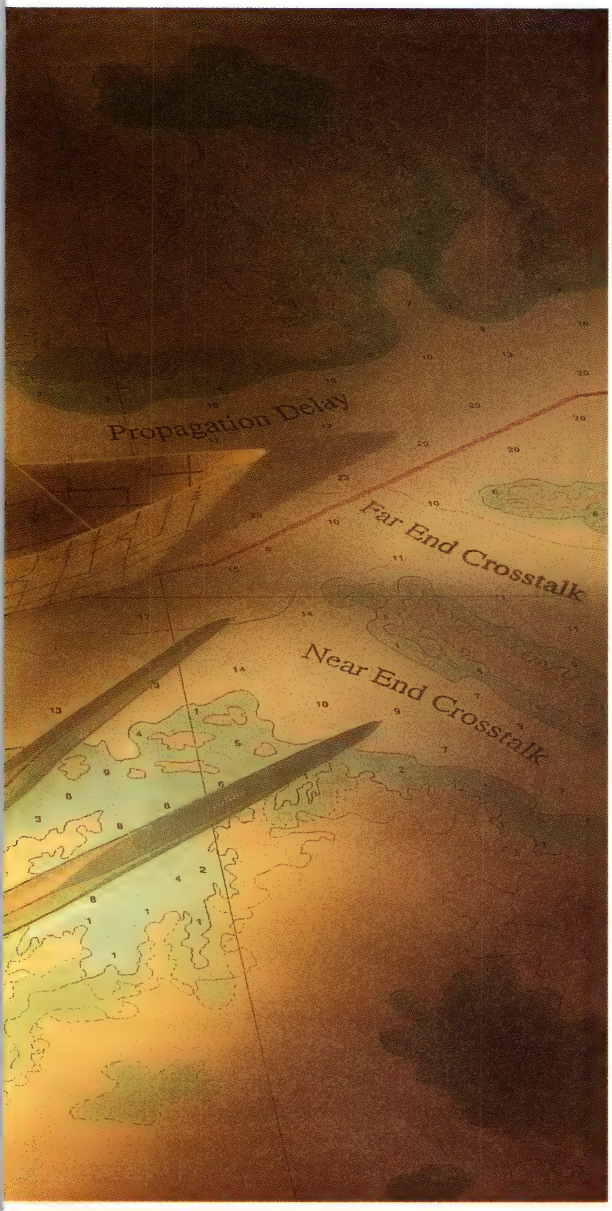


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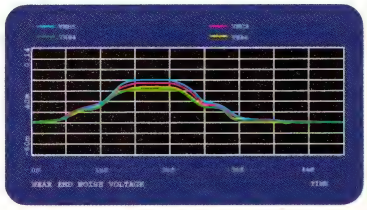

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**CIRCLE NO. 71**

# Distributed power takes center stage

**Distributed power has become a strategic architecture, if not a total solution, for digital systems. In particular, systems that need flexibility in either supply voltages or power levels benefit from distributed power, which also suits large digital systems.**

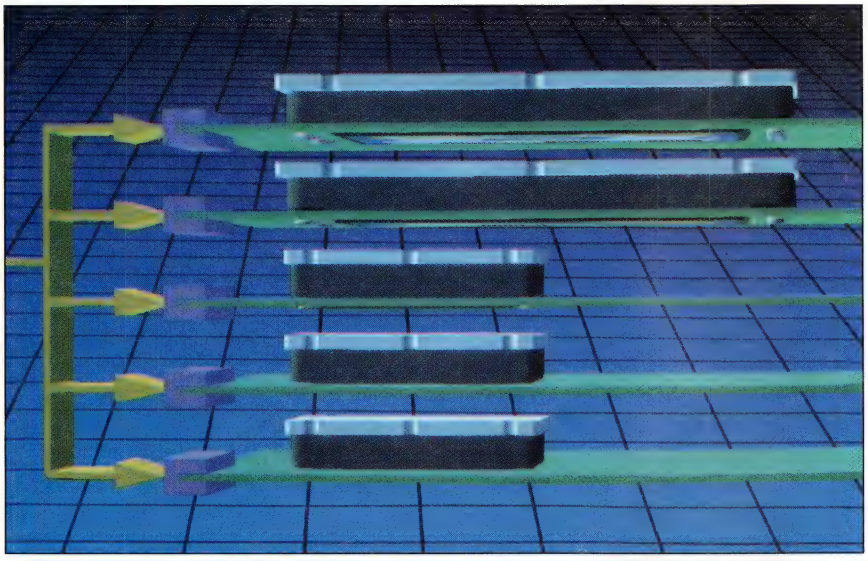
Charles H Small, Senior Technical Editor

Digital systems that in the past would have used a single, centralized-power supply now use distributed-power supplies. A distributed-power architecture is particularly attractive to several classes of digital systems. The first class is those systems that need multiple voltage levels. Also, highly configurable systems, such as workstations, can benefit from distributed power. Distributed power is not limited to just small- and medium-sized digital systems; by using distributed power, large digital systems, such as private-branch exchanges and digital telecommunications systems, can eliminate both high-current, low-voltage bus bars and the single-point failure mode of a centralized-power supply.

The term "distributed power" means that each pc board or module in a digital system has its own local dc/dc converter situated physically close to the point of load (**Ref 1**). One key factor of the attractiveness of distributed power is purely mechanical: It lets you handle distributed-power dc/dc converters as components, assembling them on your pc boards, just as you would any other component. Bulk power supplies, on the other hand, are typically large mechanical assemblies that you must install and connect separately.

Distributed power leads to a significant advantage for racked systems. Rather than distributing low voltages, such as 3 or 5V, at high current, a distributed-power system's ac/dc "bulk" converter dispenses higher voltages, such as 48 or 300V dc to its pc boards (**Fig 1**). Board-level distributed-power converters are available that accept standard telecomm, military, and industrial input-voltage levels. These higher intermediate voltages obviously result in proportionally lower currents. Consequently, conducting the lower currents requires much less copper and fewer backplane-connector pins.

Distributed-power systems have many physically smaller power assemblies than do centralized-power systems. Centralized-power systems tend to have a small number of heavy assemblies. The weight of the power assemblies is important not only in manufacturing but also in the impact on a system's resis-



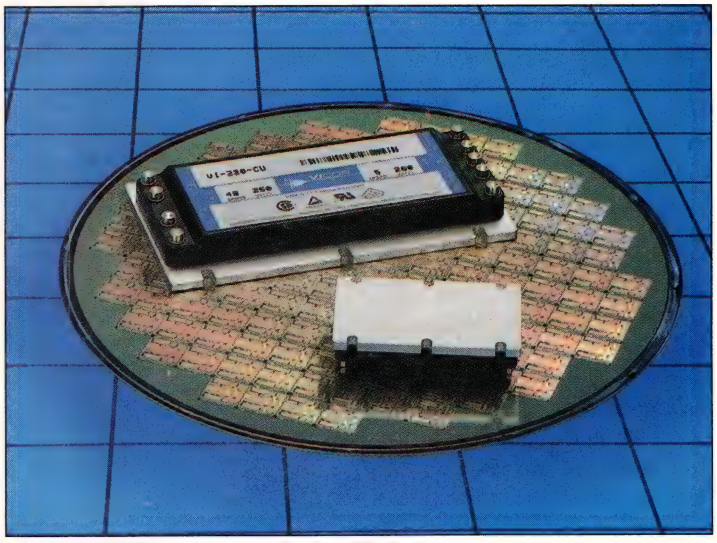
**Photographs courtesy Vicor**

tance to vibration and shock.

As the inexpensive supplies in PCs show, the hardware cost of a custom, bulk supply can be very low, but other custom-supply costs are not. A custom supply often takes a significant amount of time to design. The power supply's designer must foretell the maximum load currents the supply will encounter over the life of a product, even if the owner later installs options. While standard ICs' data sheets provide the means to estimate power consumption, such estimations for custom devices can require advanced tools, such as Systems Science's $18,500 PowerSim for VHDL ICs. Consequently, custom supplies are often overdesigned.

Any changes in requirements entail design changes. After each redesign, you must requalify the custom supply with safety agencies. If the custom power supply has a fan, the fan affects reliability because fans are a limited-lifetime component with a relatively high failure rate.

Rather than concentrate power converters and their resulting power dissipation, distributed-power systems diffuse heat throughout a system. Using distributed power, onboard converters in the 5 to 50W range can supply most loads. In these cases, natural convection can often cool the system, eliminating the use of fans. Higher loads often require forced convection. The price for poor cooling is a 50% reduction in MTBF for every 10°C temperature rise. Or, as Calex's Steve Hageman says, "If you cannot touch your design because it runs too hot, it probably isn't reliable."



Distributed power is not a new concept. Engineers have long been using DIP-sized dc/dc converters to develop tiny amounts ±12 or ±15V for RS-232C ports or small analog circuits from local 5V digital-circuit power. Even today, a less efficient—but *much* less costly—onboard linear regulator is often the best choice for deriving small amounts of power from a higher intermediate voltage. The telecomm industry is also using small, board-mounted, dc/dc converters to develop electronics voltages from standard telecomm-equipment voltages, such as 48V dc. However, these dc/dc converters are limited to specific applications.

The concept of distributed power really took off in the mid-1980s when Vicor Inc fielded high-power, compact converters in component form, and, simultaneously, the work-

station industry needed to develop highly configurable products. Vicor's early lead led to an industrywide "Vicor-standard" footprint—but, alas, not a standard pinout or any compatibility between products from different suppliers (**Fig 2**).

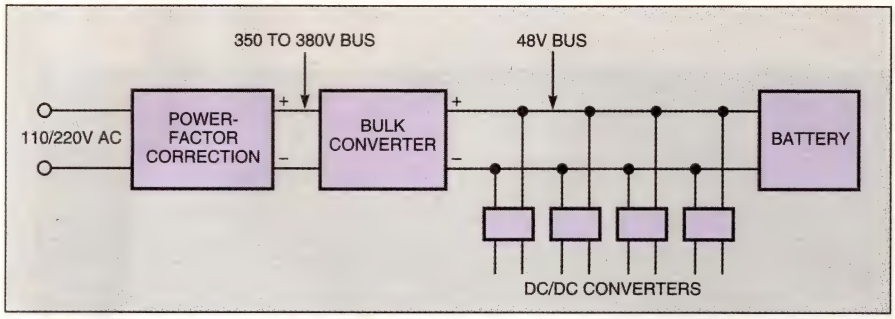



**Fig 1—A distributed-power system relies on pc-board-mounted local dc/dc converters.**

### Benefits of distributed power

Distributed power can reduce development cycles. You can select a converter for each pc board as you develop the board. The power supplies can thus be integral to your system—not an afterthought. You do not have to wait until the end of your development cycle to determine a system's power requirements all at once. A distributed-power system design is very predictable and can lead to reduced NRE costs. These savings can outweigh the distributed-power modules' higher cost. Power Micro expects 1500W distributed-power systems to cost less than $0.75/W within the next two to three years.

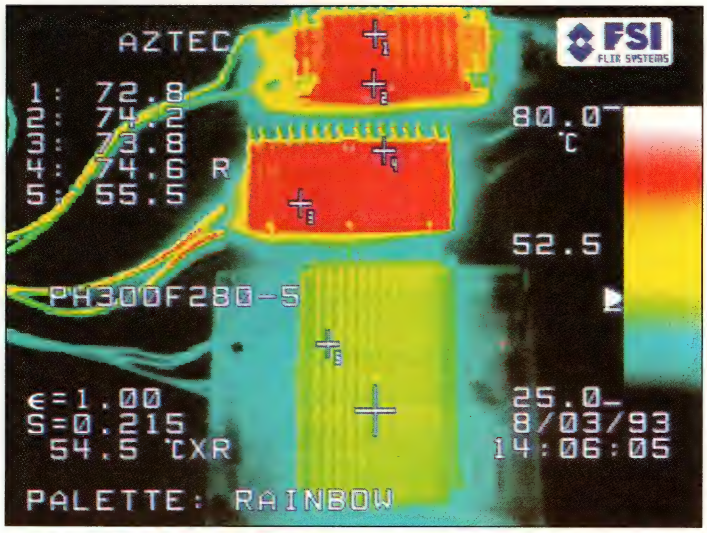
Using the 1-converter/board approach eliminates low-voltage dc distribution—except for distributing power on individual pc boards themselves, of course. In other words, you can eliminate hefty wiring harnesses and bus bars. Because a distributed-power system minimizes parasitics, it can have better transient response than that of a centralized-power system.

Upgrades are often easier, too. Consider that when you want to upgrade a system, you may want to do more than just increase the power. You may need to add a new voltage for some advanced ICs that operate from lower voltages. As part of an upgrade, you can sometimes simply swap out the local power converter rather than the whole power system. Upgrading a system having a centralized-power supply this way may not be physically possible. The pc traces and backplane connector may not have enough pins or enough power-handling capacity.

The architecture of a power system includes not only the power buses, but also power-supply control, fault diagnosis, and status reporting. Distributed-power systems obviate remote sensing along with associated reliability and diagnostic problems in most systems.

You could monitor or control a wide range of power-system elements: output voltages, airflows, temperatures, and energy saving during battery operation, among others. The most basic and useful control is turning the converter on and off with an external signal. Using such signals, you can easily accomplish power sequencing. Some accontrol panels, such as those from Pulizzi Engineering, can help you sequence your bulk supplies.

Telecomm systems often require the converter to sense its own input voltage and to turn itself off if the input voltage goes below a certain value to safeguard a battery. Some newer converters allow you to program the voltage levels at which the converter turns on or off. You could also adjust the dc/dc converters' output-voltage margins with fixed resistors and analog switches or with D/A converters.




**Board-mounted dc/dc converters are a "hot" button for today's system designers. (Photo courtesy Calex)**

### Fault isolation

You can isolate faults and contain damage more easily in a distributed-power system than in centralized-power system. You may need no more than simple board-level diagnostics. Distributed-power systems usually combine the converter with the "field-replaceable unit" (FRU) it powers. Standard engineering techniques can make pc boards and modules "hot-swappable." Thus, a service technician can simply replace the entire function and its power supply at the same time in the event of a failure (**Fig 3**). If a converter's output in a distributed-power system goes high, it damages only one pc board. If a centralized-power supply sustains an overvoltage condition, it can fry every component in the entire system.

Acceptable reliability differs, depending on whether you want a fault-tolerant or a high-availability system. By definition, no single failure ever brings down a fault-tolerant system. "Fault tolerant" implies full-blown duplication of hardware and exhaustive self-diagnostics. "High availability" means that only the rarest and most unlikely failures can bring down the system. High availability trades off availability for cost.

The most obvious potential culprit for a catastrophic, single-point failure in a distributed-power system is the ac/dc bulk converter. The probability of an output short in an ac/dc converter is very small, but not zero. Techniques used in high-availability systems to

make the ac/dc conversion less failure-prone include N+1 redundant ac/dc converters (or N+2...N+M). A fault-tolerant system would have 2N-redundant ac/dc converters.

In some cases, a pc board may demand more current than a single board-level dc/dc converter can supply while still meeting the component-height restrictions of your card cage. In such cases, consider paralleling on-board converters. You can also parallel on-board converters for N+1 redundancy.

Whether you are paralleling ac/dc converters or dc/dc converters, paralleling adds complexity to the system and typically entails accepting some performance or cost compromises. When paralleling converters, mount all the converters in a common thermal environment so that they experience as close to the same temperature as possible.

Paralleling supplies with blocking ("ORing") diodes is more reliable than simply paralleling the supplies' outputs. Run such diodes hot, and use very low forward-drop devices. After all, reverse-leakage current is an issue only on failure.

Distributed power makes hot swapping easier. Because hot swapping a module of a distributed-power system affects only a small portion of the total power, "glitch-free" swaps are easy to ensure. Hot swapping can be a big advantage for large systems that must remain continuously on-line. Blocking diodes also simplify hot swapping.

If you step back and take a systemwide view, you will see that a distributed-power architecture duplicates many power-supply circuit elements. In a distributed-power system, each converter has its own control and fault-handling circuitry. In a bulk-supply system, the bulk-supply has only one of each of these elements.

Given that increasing the number of components decreases reliability, distributed-power makers have had to increase the reliability of their dc/dc converters. For example, Vicor has demonstrated MTBF of greater than 20 million hours. However, not all converter makers have taken the time to characterize their products over such long periods. Consequently, you often have no choice other than to rely on *calculated* MTBF.

Although telecomm standards exist for calculating MTBF, most power-supply vendors use MIL-HDBK-217 instead. Even though this practice is widespread, MIL-HDBK-217 has its problems; it depends on a database of component types and their field-failure rates. This database focuses on military components and takes time to accumulate. As a consequence, most newer commercial technologies are *not* available in the database.

MIL-HDBK-217 imposes a harsh—and possibly unjustified—penalty on nonmilitary components. Further, some of its component-failure rates are not consistent with those components' actual performances. For example, transformers and magnetic devices have a very low actual failure rate, but MIL-HDBK-217's predicted rate for these components is very high. ICs fare even worse than do magnetic components.

At least two converter companies have compared MIL-HDBK-217's predictions to the actual field performance of their dc/dc converters. Ericsson finds that its converters run 3 to 10 times longer than MIL-HDBK-217 predicts, while Vicor sees two to three times longer performance.

To select your intermediate-bus voltage, first consider the ease of safety approval vs cost. A lower voltage entails more expense to handle the higher currents, but the lower voltage may be more acceptable to regulatory agencies.

Every country has some kind of safety standard or requirement that limits the maximum voltage to which you can expose equipment operators and service personnel. The common term for this limit is "safety extra-low voltage" (SELV), but not all agencies set SELV at the same level. The most commonly accepted value for SELV is slightly more than 60V. Consequently, if your intermediate bus voltage is less than 60V, your product more easily complies with safety shielding and regulations.

However, your nominal intermediate-bus voltage has high and low limits for conditions such as battery charging and load switching. For the 48V-dc telecomm standard, for example, the maximum voltage is 60V—very close to the most generally accepted SELV limit. Therefore, a nominal 48V is currently the highest SELV for a distributed-power system's intermediate voltage.

But you could follow the example of mainframe-computer makers, rectifying and filtering the ac line to yield 300V-dc intermediate voltage. This

## TABLE 1—TEMPERATURE DEFINITIONS

| Parameter | Description |
|---|---|
| Ambient temperature | Air temperature external to power converter; higher than environmental temperature because of heat dissipation within the system's enclosure; used for free- and forced-convection cooling. |
| Case temperature | Temperature of the case of the power converter; used for free- and forced-convection cooling as well as conduction cooling if the case is the principal thermal path. |
| Component-core temperature | Temperature of the interior of a component; used for all methods of cooling. For semiconductors, equal to the junction temperature, $T_j$. |
| Component-surface temperature | Temperature of a component within the power converter, measured at the component's external surface; used for all cooling methods. |
| Environmental temperature | Air temperature to which a system is exposed; used in all cooling methods; for systems installed indoors, equal to room temperature. |
| Heat-sink temperature | Average temperature of a heat sink attached to the power module; typically slightly lower than the case temperature. Used for all types of cooling if heat sink is present. |
| Pin temperature | Average temperature of the power converter's pins; very close to the temperature of the circuit board on which the converter is mounted; used for conduction cooling when the module pins are the principal cooling path. |

(Courtesy Ericsson)

scheme reduces the cost of both the ac/dc converter and the intermediate-voltage distribution. Your genuine safety concerns for a high-voltage bus are creepage and clearance, preventing access to shock hazards, and large amounts of stored energy available to short circuits.

If the load on the intermediate-voltage bus switches rapidly, such as when a fuse opens, the bus's inductance can generate a voltage pulse having as much as 70 Wsec of energy.

For a 300V intermediate bus, overload and short-circuit protection require large devices to handle inrush and arcing. However, there is a dearth of standard connectors and fewer standard converters for 300V. And backing up a 300V bus with a battery obviously requires more cells than does backing up a 48V bus.

You need to carefully consider overcurrent protection for the intermediate bus. Two common problems are that start-up requires large currents to charge the bus's capacitance. This large charging current means that the overcurrent-protection circuits can trip at start-up. The result is that the system never actually gets started. In this case, you must sequentially enable load converters only after bus voltage is stable.

You must also carefully choose your board-level converters' overcurrent protection. For example, in a battery-backed system, the constant-power nature of the load could trap a brick-wall-limiting converter at a point beyond the knee of its overcurrent characteristic.

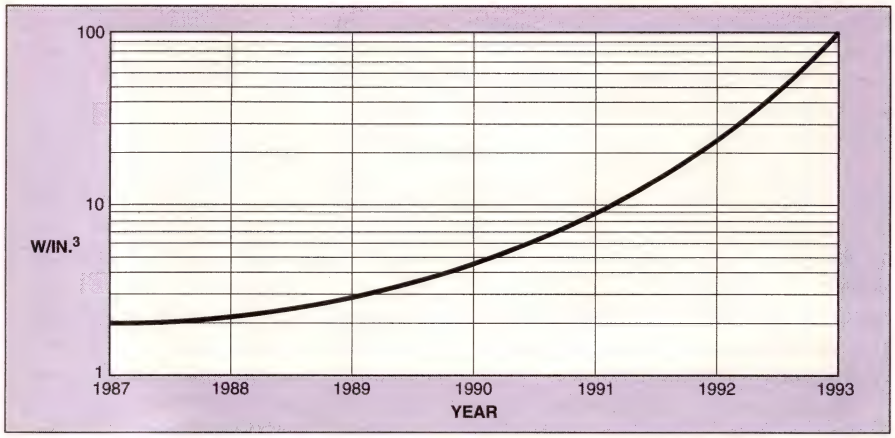



**Fig 2—Since the mid-1980s, power-supply makers have made remarkable progress in shrinking pc-board-mounted dc/dc converters.**

Opinions differ about the relative prevalence of low- and high-voltage intermediate-bus distributed-power systems. According to Ericsson, most distributed-power systems have bus voltages below the SELV limit. Vicor, on the other hand, sees a 50:50 distribution between 48 and 300V systems.

You can opt for isolated and nonisolated dc/dc converters. Isolated converters are more expensive but are also safer, and they reduce problems with system noise, ground loops, and interaction between outputs. In addition to operating from either polarity of input voltage, isolated converters permit flexible system grounding.

In a centralized-power system or a distributed-power system using nonisolated converters, the common of the power-distribution system is also signal common. The common of the power-distribution bus is isolated from signal commons in distributed-power systems using isolated dc/dc converters.

No engineer runs dc/dc converters continuously at their rated full load. Ericsson reports that most designers allow margins of 15 to 40%. The penalty for under-margining is obviously more extreme than that for over-margining. The power-supply margins are easier to determine in a distributed-power system.

**TABLE 2—DESIGN TRADEOFFS**

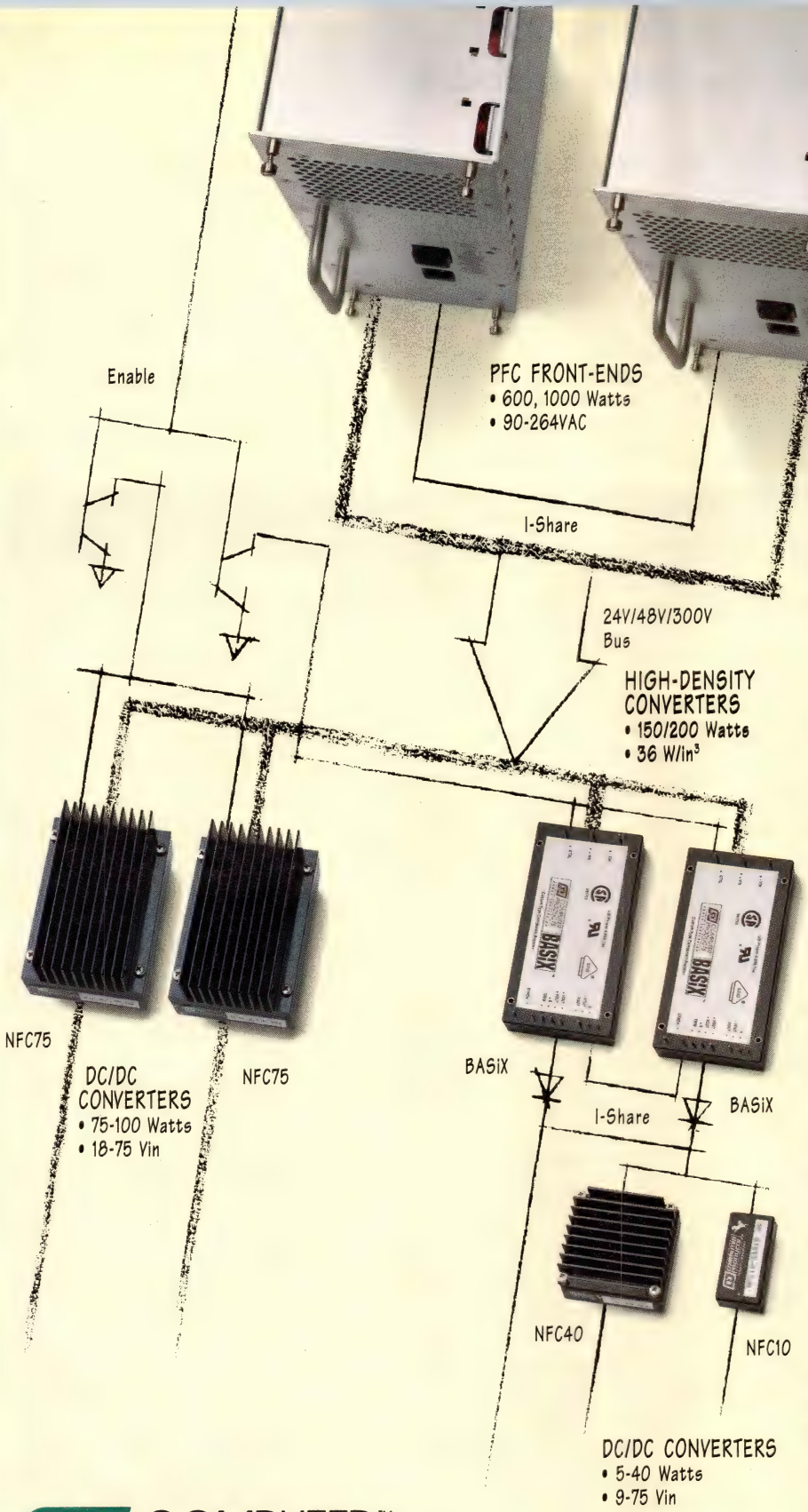
| | Conduction | Free convection | Forced convection |
|---|---|---|---|
| **Typical module usage** | Low power, board mounted | Low to medium power, board mounted | Medium or high power, board mounted or centralized |
| **Advantages** | Low cost, high reliability, ease of thermal analysis, not orientation-sensitive | Low cost, high reliability | Higher density |
| **Disadvantages** | Limited supplier selection | Low density, orientation sensitive | Less reliable, more complex, field service required, more costly |
| **Design tradeoffs** | Reliability, efficiency, maximum pin temperature | Reliability, efficiency, board area, maximum case temperature | Reliability,efficiency, board area, airflow, maximum case temperature |

(Courtesy Ericsson)

### Constant vs variable frequency

Each converter manufacturer has its own circuit topology. Some employ constant-frequency converters that use PWM for voltage control. Vicor uses a variable-frequency resonant scheme. According to Vicor, the efficiency of PWM converters is usually lower than that of similar-capacity resonant converters. Vicor also notes that a PWM converter's efficiency drops rapidly with load, culminating with high dissipation under output short circuit. The company also states that PWM converters emit difficult-to-filter conducted and radiated common-mode (Denkaplate), normal-mode, and radiated noise and that their output ripple increases with load.

PWM-converter makers, however, have been busy enhancing their designs. So your best guides are spec sheets and your own tests. However,

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make sure your quality-assurance staff is not using outmoded tests designed for linear supplies (see **Ref 2** for proper setups). Test your candidate converters in a realistic circuit.

A converter's operating frequency *is* important, however, because it determines the time required to sense and respond to a change in load current. The converter's topology and circuit design set a limit for the amount of energy delivered to the load per converter operating cycle. A converter may take several operating cycles to meet a demand for dynamic current.

You can synchronize many converters, but AT&T questions this practice. The fear is that two units operating at nearly the same frequency will "beat" and produce extraneous emissions. But synchronizing makes emissions worse because it causes all the converters' emissions to add arithmetically. Without synchronization, the reflected currents add in rms fashion.

You must look very closely at efficiency. Small size combined with low efficiency spells disaster. The higher the efficiency, the higher the MTBF for both the converter and the system. Also, high efficiency extends backup-battery holdup time. Efficient converters permit the use of smaller heat sinks and quieter fans.

Converter efficiency is a family of curves, not a single figure. So, look at

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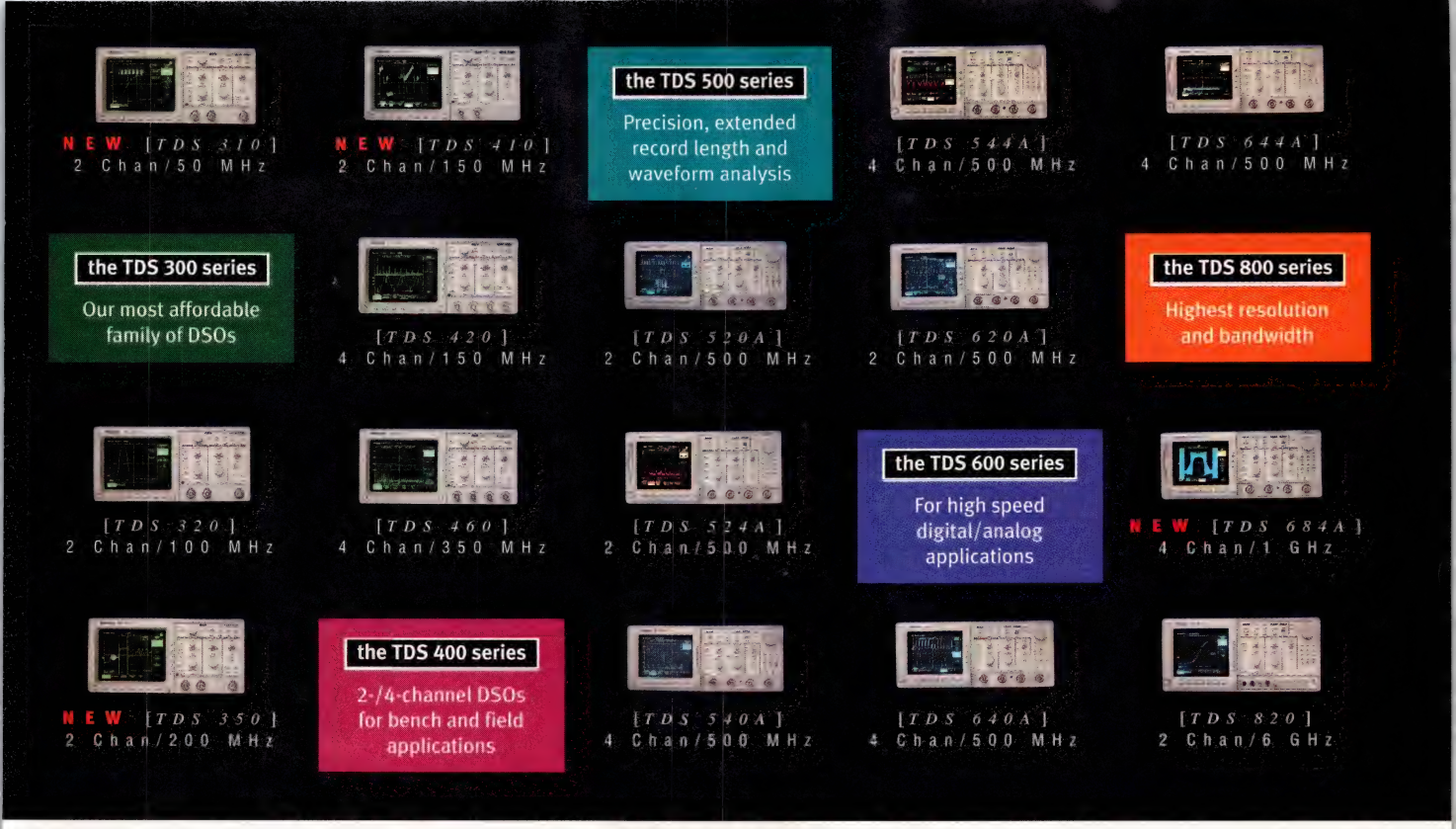


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CIRCLE NO. 74

efficiency across both line and load variations. For safety's sake, also look at dissipation under short-circuit conditions.

Efficiency for dc/dc converters currently ranges from about 75 to 83%. At first glance, this small range may appear to be meaningless, but it is actually a very significant difference because converting differences in percentages into percentage differences is not intuitive. A 75%-efficient converter dissipates 60% more power at full load than does an 83%-efficient converter. Politicians take advantage of this weakness in human intuition when they call an increase in taxes from 5 to 6% a "1% increase" (when it's really a 20% increase).

Advertised power levels for dc/dc converters are often very optimistic. Don't neglect the fine print, which says that the converters need heat sinks to achieve their advertised performance. Also note at what ambient temperature the converter needs derating. Converters from different manufacturers exhibit a wide range of ambient-temperature operation. "Ambient temperature" means different things to different manufacturers. See **Table 1** for temperature definitions.

Ericsson finds that distributed converters have 3 to 11 times the power density of the pc board they occupy. That is, converters are a concentrated source of heat. Ericsson recommends, therefore, for free convection the converter can occupy no more than about 2% of the pc board's area and that for forced convection, the converter can occupy no more that about 7% of the pc board's area.

Only converters at both extremes of the power range use conduction for cooling (**Table 2**). Mainframe-computer converters that supply hundreds or even thousands of amps use a recirculating coolant. At the other extreme are low-power converters, 10W or less, that conduct heat out through their leads.

Convection cooling is more difficult to model and analyze than is conduction cooling. Free-convection cooling is very simple and reliable. Also, convection cooling does not entail the acoustic noise, maintenance, cost, and degraded reliability that fans introduce. However, many systems require fans because forced convection can cool about four times the power per board compared with free convection.

Opinions differ on filtering. Both Ericsson and Vicor say that you do not need to use a filter at the input of the dc/dc converter if you have properly designed and executed your dc distribution and decoupling. Datel, on the other hand, says most of its customers want such filters. Datel adds that engineers are specifying IEC noise limits for dc/dc converters (but not, of course, the IEC test setup because the spec actually applies to ac-line noise).

Selecting ac/dc converters for distributed-power systems is much like selecting any ac-input supply. You need to decide if you want manually strapped or autoranging inputs for single- or 3-phase mains voltages. Even with power-factor correction, many systems are already drawing the maximum amount of current allowable from a single-phase connection (**Table 3**). Power-factor-correcting ac/dc converters are also becoming more common as regulatory agencies tighten up on conducted noise. One more hint: Look for ac/dc supplies that require no preload.

**TABLE 3—AVAILABLE POWER VS GEOGRAPHICAL AREA**

| Area | Voltage | Current | Max VA | Max 48V (W) |
|---|---|---|---|---|
| North America | 120 | 15 | 1800 | 1183.3 |
| | | 20 | 2400 | 1560.2 |
| | 208 | 15 | 3120 | 2066.2 |
| | | 20 | 4160 | 2737.4 |
| United Kingdom | 240 | 10 | 2400 | 1597.7 |
| | | 13 | 3120 | 2072.5 |
| Continental Europe | 220 | 10 | 2200 | 1464 |
| | | 16 | 3520 | 2329.9 |
| Japan | 100 | 15 | 1500 | 982.8 |
| | | 20 | 2000 | 1292.9 |
| | 200 | 15 | 3000 | 1985.9 |
| | | 20 | 4000 | 2630.4 |

(Courtesy AT&T)

**Problems with distributed power**

One major problem with distributed power is that the most frequently promoted spec for dc/dc converters, power density, is also the most useless. Fantastic power densities tend to wilt after you expose them to the harsh glare of your application's environment. You can compare power densities of different makers' dc/dc converters only after taking into account heat sinks, derating, and other design considerations. Fully configured, some high-density dc/dc converters are large and heavy enough to damage their host pc board during shipping and usage.

Next, the switch to a 3.3V digital standard is not as easy as just swapping out converter modules. If you are to take the JEDEC standard seriously, its ±0.1V tolerance means that a μP drawing 4A could have no more than 0.025Ω trace resistance between itself and its dc/dc converter. In other words, a fine trace or a connector can put you out of spec. Also, noise currents in the system ground can quickly eat up 3.3V noise margins. If you have a mixed-voltage board, carefully check your margins for the worst-case supply condition: 3.3V supplies at their high end (3.4 or 3.6V)

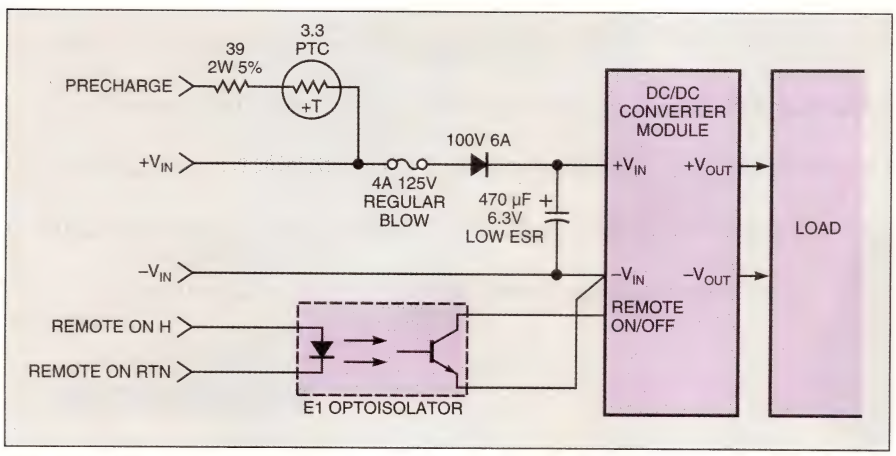


**Fig 3—AT&T suggests this circuit for making a pc board "hot swappable."**

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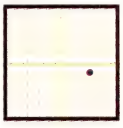

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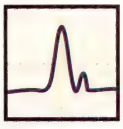

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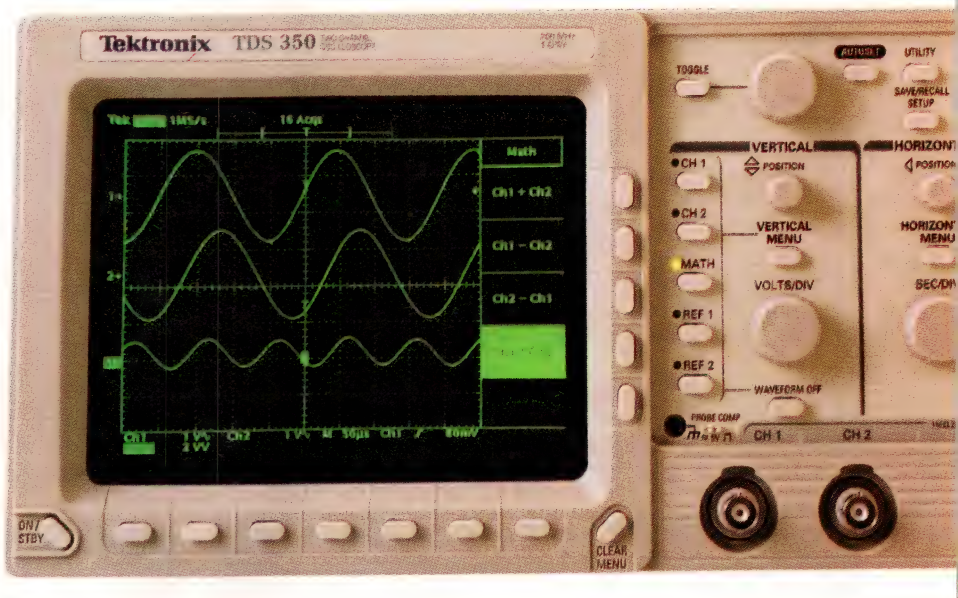


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CIRCLE NO. 73

## DISTRIBUTED POWER

and 5V supplies at their low end (4.75 or 4.5V). You might be in for a nasty surprise if you are interfacing 3.3 and 5V ICs.

Although JEDEC has promulgated a 3.3V standard, little actual conformance exists in the industry. Various manufacturers are going ahead with low-voltage standards other than 3.3V. Semtech notes that on mixed-voltage boards, you might have to be very careful how you sequence your supplies up and down to avoid failures. The company also notes that transient-voltage-protection devices for 3.3V circuits are rare.

At the new, lower voltages, large current surges can occur on the pc board itself. So-called "green" PCs (which switch large digital devices on or off as needed) and low-voltage disk drives are two possible sources of such surges. These surges may necessitate remote sensing for board-mounted converters, reintroducing a problem that distributed power supposedly eliminates (**Fig 4**). Further, the digital ICs themselves may be drawing pulsed currents at a high enough frequency that the skin effect may come into play in their power and ground lines. EDN

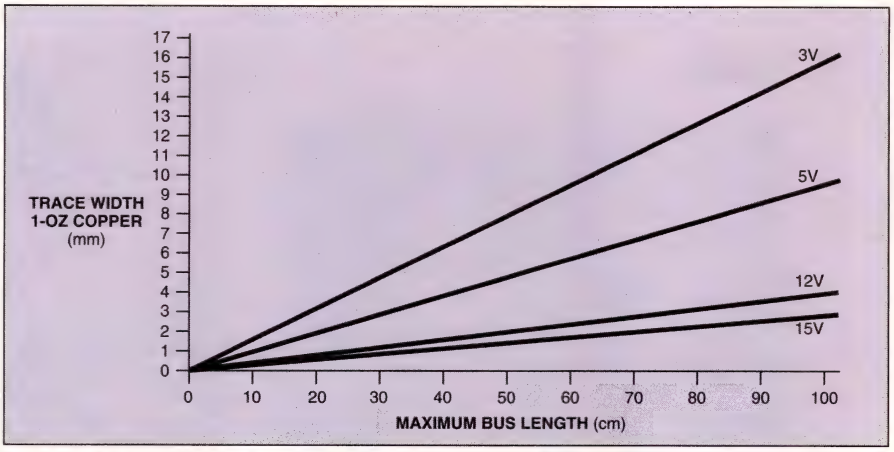


**Fig 4—High-current, high-frequency ICs may so tax the current-carrying capacity of pc-board traces that even distributed-power systems may have to resort to remote sensing.**

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2. Hageman, Steven C, "DC/DC Converter Application Notes," Calex, Concord, CA.

3. "Applying DC/DC Converters," Conversion Devices Inc, Brockton, MA.

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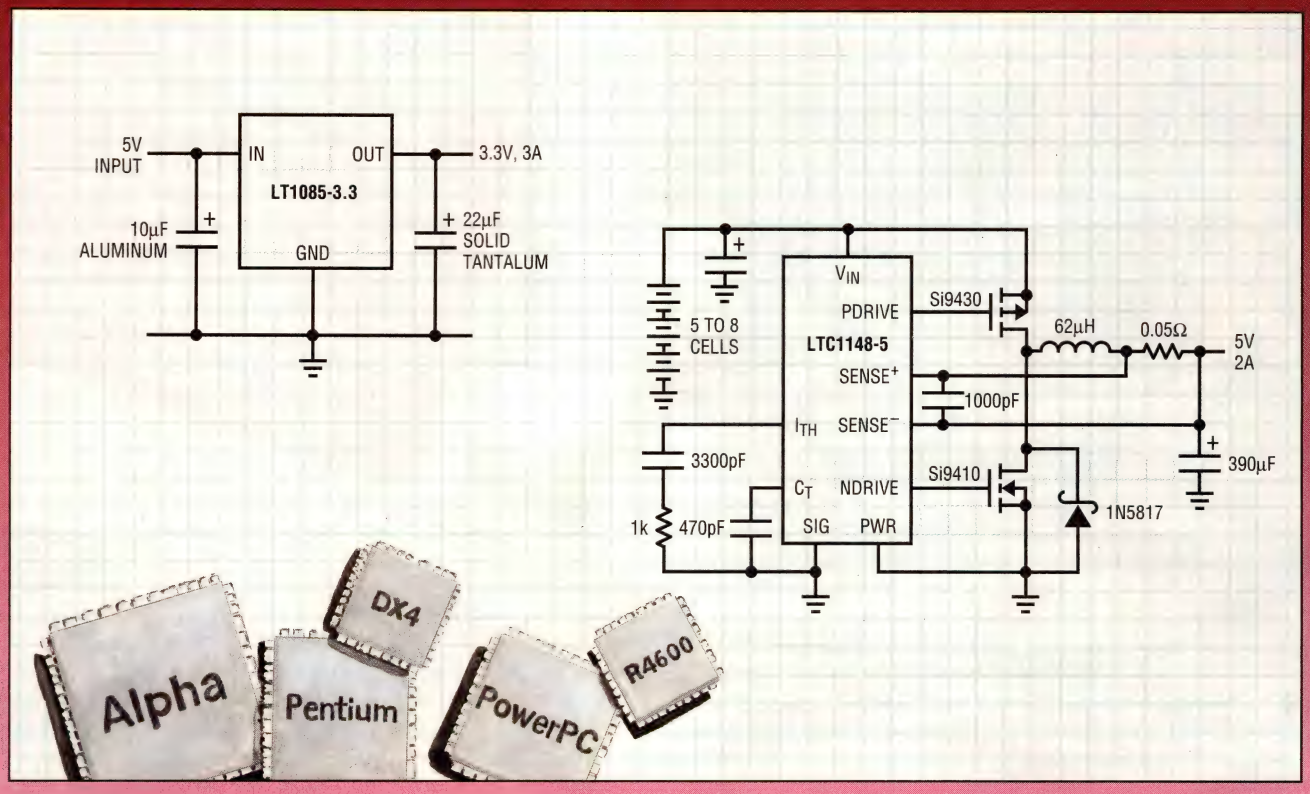
CIRCLE NO. 75

# 5V→3.3V: Linear or Switcher?




You have chosen your processor, now you must choose your power supply. Linear Technology provides you with the best solutions, linear regulator or switching regulator to convert from 5V to 3.3V at any current. We also allow you to tailor your output from 2.9V to 3.6V.

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| Output Current | Linear Regulator | Switching Regulator |
|---|---|---|
| 1.5A | LT1086-3.5 | LTC1147-3.3 |
| 3A | LT1085-3.3 | LTC1148-3.3 |
| 5A | LT1084-3.3 | LTC1148-3.3 |
| 7.5A | LT1083 | LT1158 |
| 10A | LT1087 (X2) | LT1158 |
| 15A (20A Peak) | N/A | LT1158 |

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CIRCLE NO. 76

# Composite amp provides high gain and bandwidth

**Mark Sauerwald, Comlinear Corp, Ft Collins, CO**

The composite circuit in **Fig 1** couples the output drive and slew rate of a current-feedback amplifier, $IC_2$, with the low-noise and low-offset characteristics of a voltage-feedback operational amplifier, $IC_1$. The circuit achieves gains as high as 1000, while showing little variation in frequency characteristics with gain. This circuit suits applications requiring high gain and wide dynamic range, such as ultrasound, radar, digital radio, and other high-noise applications.

$IC_1$ has a gain-bandwidth product of approximately 1.6 GHz. Configured as an amplifier with a gain of 1000, it would exhibit less than 2 MHz of bandwidth. Further, the limit of the output swing of $IC_1$ is less than ±3.8V typ. $IC_2$ has over 50 MHz of bandwidth and ±13V output swings along with the gain-bandwidth independence for which current feedback is famous. Unfortunately, current-feedback amplifiers are not suitable for very high gains. To achieve high gain, a current-feedback amplifier's gain-setting resistor must become very small (for gain-bandwidth independence, the feedback resistor must remain relatively constant), and the signal gets lost in the current-feedback amplifier's noise.

In **Fig 1**, $IC_1$ has a gain of 1000 and is inside $IC_2$'s feedback loop. $IC_2$ is a gain block with A=10. Thus, $IC_1$ is actually providing a gain of only 100, allowing it to maintain in excess of 10 MHz of bandwidth and requiring it to develop relatively small output swings.

Because $IC_2$ has a gain of only 10, it has reasonable gain-resistor values, and their noise contribution is not significant. For this circuit to remain stable, $IC_1$ must have sufficient phase margin to allow for $IC_2$'s phase lag. Adding the resistor from $IC_1$'s $R_P$ pin to $V_{EE}$ reduces the current $IC_1$ draws, compensating the amplifier. A 250Ω resistor stabilizes the circuit, allows for a 10-MHz large-signal bandwidth, and still offers good gain flatness.

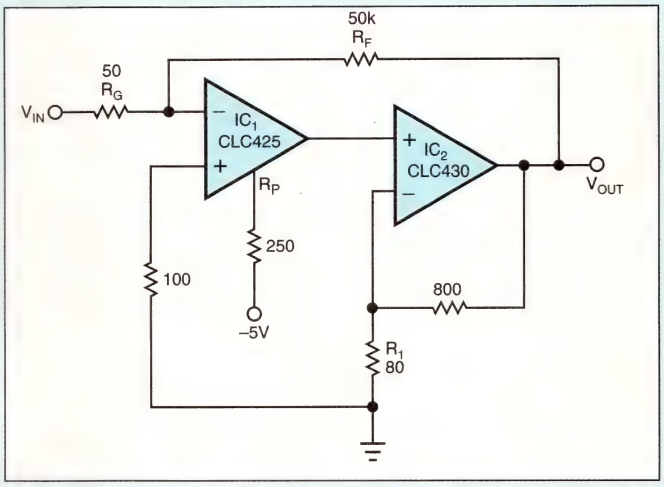


**Fig 1—Combining current-feedback and voltage-feedback amplifiers yields a composite amplifier having high gain and wide bandwidth.**

If you need similar frequency characteristics at another gain, change the gain of $IC_2$. The current-feedback amplifier's frequency characteristics are independent of gain. For example, to reduce the circuit's gain to 500, reduce $R_F$ to 25 kΩ and increase $R_1$ to 160Ω, so that $IC_1$'s gain is still 100. Increasing gain simply by increasing $R_F$ proportionally decreases the circuit's bandwidth. (DI #1399) EDN

**To Vote For This Design, Circle No. 472**

# Passive differentiator tops active designs

**Stan Bleszynski, Applied Micro Electronics Ltd, Dublin, Ireland**

The simple, passive differentiator in **Fig 1** achieves accurate differentiation even at frequencies approaching the limit, $f_0=1/(2\pi RC)$. The circuit surpasses the performance of an op-amp-based differentiator. The trick is to add a carefully selected inductor, L, to eliminate the first- and second-order terms in the equation for the phase angle, ϕ, between the input and output signals. Ideally, of course, to achieve perfect differentiation, this phase angle should be equal to 90° (ie, $\cot(\phi)=0$), regardless of the frequency, f.

$$(\cot(\Phi))^2=\left(\frac{f}{f_0}\right)^2\left(1-\frac{f_0}{f_1}\right)^2+\left(\frac{f}{f_0}\right)^4\left(1-\frac{f_0}{f_1}\right)2\left(\frac{f_0}{f_1}\right)^2+\left(\frac{f}{f_0}\right)^6\left(\frac{f_0}{f_1}\right)^4$$

where $f_0=1/(2\pi RC)$ and $f_1=R/(2\pi L)$.

You force the first two error terms to vanish by first calculating R and C to satisfy requirements for the circuit's input impedance, such that $f_0$ is at least two to three times the maximum signal frequency the circuit will encounter. Then, set $f_1=f_0$; that is, $L=R^2C$. The phase error thus reduces to $\cot(\phi)=(f/f_0)^3$, which remains quite small even for frequencies comparable to $f_0$. (DI #1400) EDN

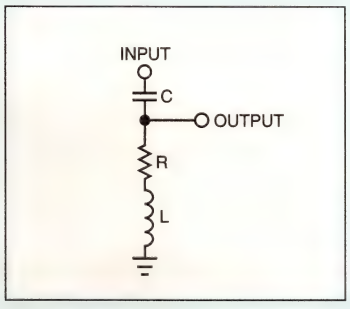


**Fig 1—With properly selected components, this simple passive differentiator can beat the performance of an op-amp differentiator.**

**To Vote For This Design, Circle No. 473**

# 3½-digit DVM IC measures power factor

**Devadoss John and KRS Sarma, Hindustan Cables Ltd, Hyderabad, India**

The circuitry in **Fig 1** allows the ICL7106/7107 digital-voltmeter IC, $IC_4$, to measure power factor to 0.1% resolution and operate from a single 9Vdc supply. An important feature of the circuit is that variations in load current, line voltage, and line frequency do not affect measurements. For inductive loads, power-factor measurements are accurate to 1% in the range of 0.85 to 1.

The circuit derives two dc voltages, $V_M$ and $V_M\cos\Theta$, that go to the REF HI and IN HI inputs of $IC_4$, yielding the power factor ($V_M\cos\Theta/V_M$). A unity-gain follower, a precision rectifier ($IC_{1A}$ and $IC_{1B}$), and an RC filter obtain $V_M$ by rectifying the waveform from the secondary winding of the voltage transformer, $T_1$.

A synchronous detector ($IC_2$ and $IC_3$) derives $V_M\cos\Theta$. The current transformer, $T_2$, provides the waveform, $v(t)=kI_0\sin(2\pi ft\pm\Theta)$. Buffer $IC_{1B}$ squares this waveform, deriving control waveforms for the synchronous detector. The synchronous detector operates on the output of the input-voltage follower, $IC_{1A}$, yielding a dc output equal to $V_M\cos\Theta$. (DI #1403) EDN

**To Vote For This Design, Circle No. 474**

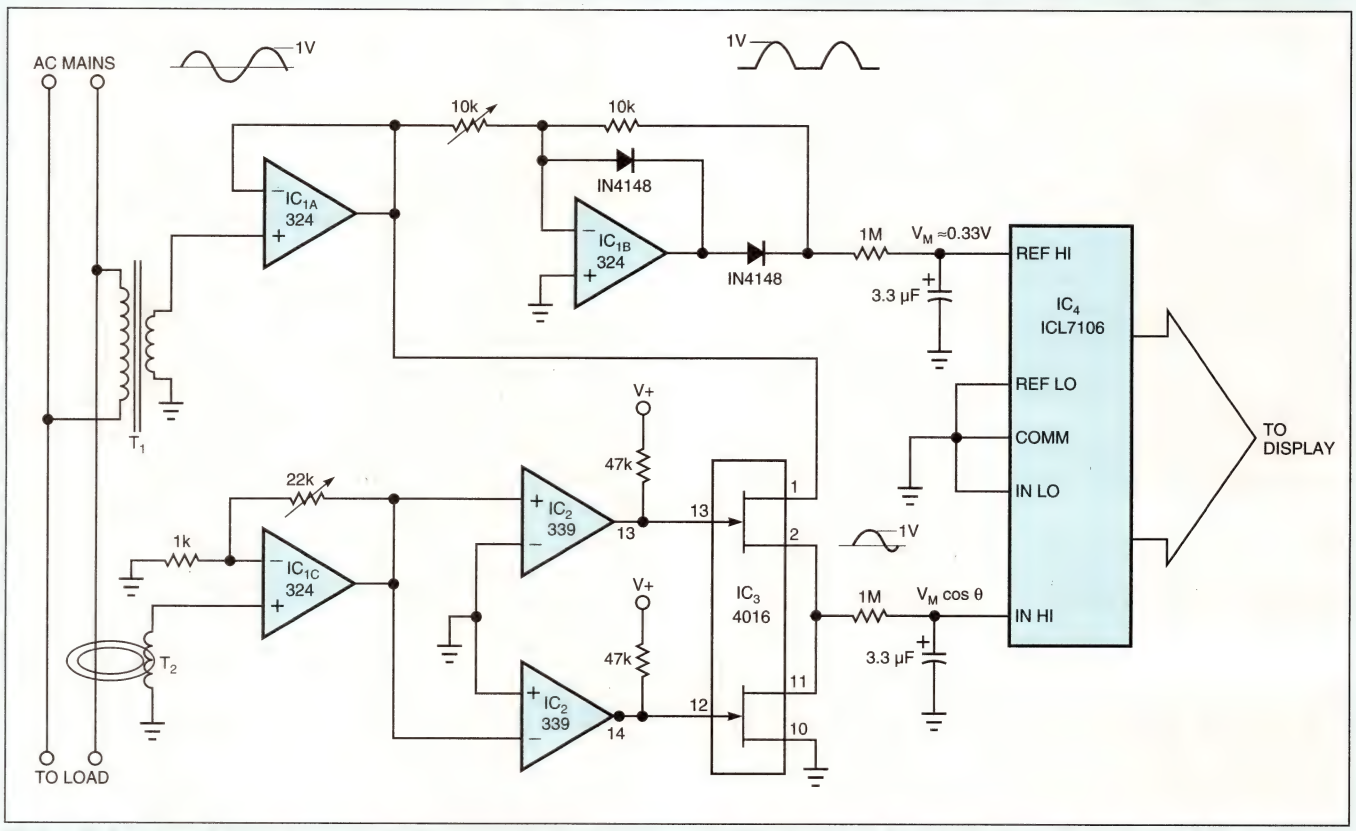


**Fig 1—A clever synchronous detector in this circuit extracts phase-angle information so that a digital-voltmeter IC can directly measure power factor.**

# 2-channel ADC tags its own output

**Fred Hamilton, National Semiconductor, Santa Clara, CA**

BBS Transferring converted data from high-speed DACs directly to system RAM to avoid µP bottlenecks is common. But, if the ADC serves more than one input, the µP obviously won't be able to select channels during the DMA period.

The circuit in **Fig 1** shows a simple way to operate a 1-MHz, 12-bit ADC ($IC_1$) in DMA mode while alternating between its two analog-input channels. The converter operates continuously, driven by the 1-MHz clock on the S/H input.

Tying RD and CS low ensures that data are always present on the ADC's output bus. The outputs of the 74HC74 flip-flop, $IC_2$, change state on the rising edge of the end-of-conversion (EOC) signal. The flip-flop's Q drives the ADC multiplexer's

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|---|---|---|---|---|---|---|
| Frequency (MHz) | dc-500 | 500-2000 | 2000-5000 | dc-500 | 500-2000 | 2000-5000 |
| Ins. Loss (dB) | 1.1 | 1.4 | 1.9 | 0.9 | 1.3 | 1.4 |
| Isolation (dB) | 42 | 31 | 20 | 50 | 40 | 28 |
| 1dB Comp. (dBm) | 18 | 20 | 22.5 | 20 | 20 | 24 |
| RF Input (max dBm) | —— | 20 | —— | 22 | 22 | 26 |
| VSWR "on" | 1.25 | 1.35 | 1.5 | 1.4 | 1.4 | 1.4 |
| Video Bkthru (mV,p/p) | 30 | 30 | 30 | 30 | 30 | 30 |
| Sw. Spd. (nsec) | 3 | 3 | 3 | 3 | 3 | 3 |
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address line (pin 16), and the flip-flop's Q output provides an output bit indicating the current channel. The memory stores this bit along with the 12-bit conversion value.

Because the address changes on the rising edge of the EOC signal, the change occurs well within the ADC multiplexer's setup-and-hold limits. The two 74HC541s isolate the ADC from the system's data bus.

Posted as **EDN BBS /DI_SIG #1412** on the EDN readers' bulletin-board system is a compressed ZIPfile containing a detailed design writeup and a PLD program for burning the circuit into a PAL16HD8. (DI #1412) EDN

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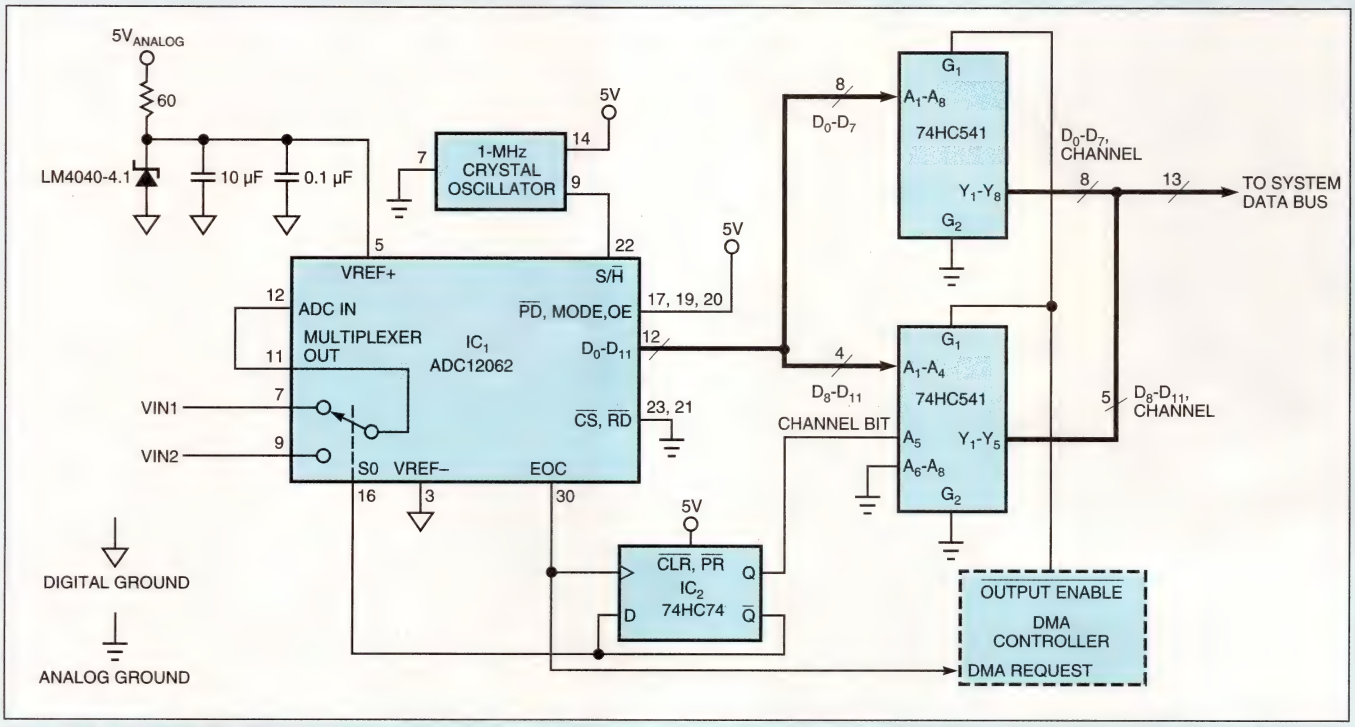


**Fig 1—The 74HC74 flip-flop controls a 2-channel ADC's input multiplexer and provides an extra memory bit that identifies which channel a sample came from.**

# Asynchronous circuit latches safely

**Paul A Kemp, NASA Johnson Space Center, Houston, TX**

BBS The circuit in **Fig 1** is a digital latch that is resettable only after the condition that set the latch clears. A set input (active low) permanently latches the output (active low). A reset input (active high) resets the output to a logic high.

Unlike the 74279 set-reset latch, you can drive the set and reset lines low simultaneously. A 74279's output is unpredictable and unstable when you drive both its set and reset lines low simultaneously. In contrast, this circuit's output remains in its present state.

The circuit operates asynchronously and can handle both the set and reset inputs' changing state simultaneously. Applications include any circuit requiring a latch that will not reset until reaching a "safe" condition. A safe condition occurs when the set line has gone low and the reset line goes high. **EDN BBS /DI_SIG #1413** contains an extensive write-up of this Design Idea's derivation. EDN

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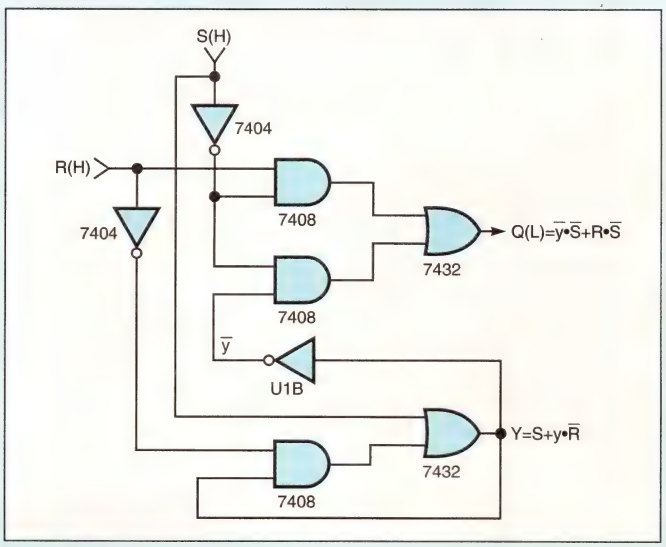


**Fig 1—This circuit is a digital latch that is resettable only after the condition that set the latch clears.**

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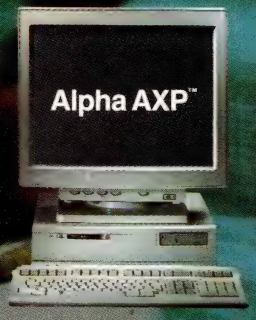


Putting Imagination To Work

digital

# Comparator improves regulator's efficiency

**Cristophe Basso, European Synchrotron Radiation Facility, Grenoble, France**

The UC384X family of current-mode PWM regulators requires a current shunt or some other component to develop a voltage proportional to the output current. This shunt must develop a 1V signal at full load.

For off-line supplies, the 1V requirement is not hard to meet because of the high voltage on the supply's dc bus. However, if you want to use a UC384X regulator in a low-voltage circuit, the 1V drop becomes undesirable. Lowering the shunt's value is not a good idea because the maximum current would rise to an unacceptable value in short-circuit or overload conditions.

The circuit in **Fig 1** shows an 11W current-mode flyback converter. An external low-offset comparator, $IC_{2A}$, overrides the output of regulator $IC_1$'s error amplifier. The $R_4$-$R_5$ network reduces the output of $IC_1$'s error amplifier and determines the maximum output of the supply. Because of the low offset of $IC_{2A}$, you can set a threshold as low as 200 mV and then employ shunts of a few tens of millohms.

$R_2$ and $C_2$ filter the output of the shunt $R_1$. The output then goes to the noninverting input of the comparator. In this design, $IC_1$'s internal comparator works simply as a switch to reset the internal latch and no longer imposes its threshold value of 1V.

The circuit develops a primary peak current of about 5.2A (2.2A rms). To provide a contrast to the comparator version, we built a version having a 0.22Ω shunt. The shunt dissipates more than 1W, dropping efficiency to less than 80%. The efficiency of the comparator version, using a 0.005Ω shunt, is more than 88%.

In this application, the low operating frequency of the supply (33 kHz) permits using a slow comparator. In higher-frequency applications, replace $IC_2$ with a faster device. You can also use this comparator technique with a sense FET because the converted voltage delivered by its current mirror does not correspond directly to the internal threshold of the UC384X. (DI #1417) EDN

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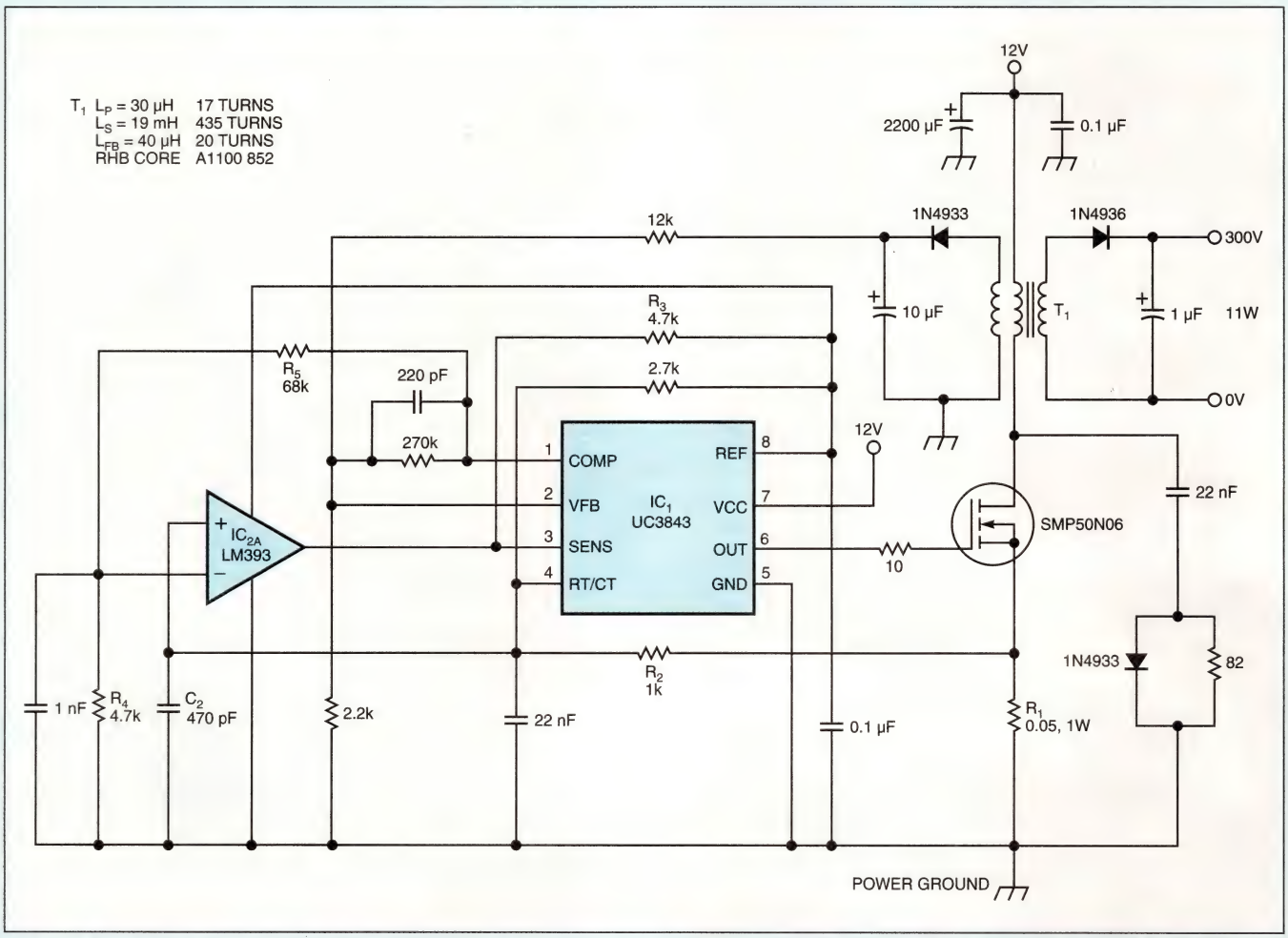


**Fig 1—In this 11W current-mode flyback converter, an external low-offset comparator, $IC_{2A}$, overrides the output of regulator $IC_1$'s error amplifier. This technique allows you to use a significantly lower-value current-sense resistor, boosting efficiency from 80 to 88%.**

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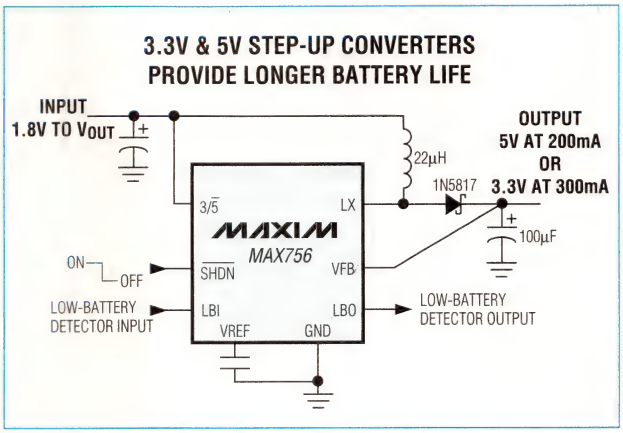


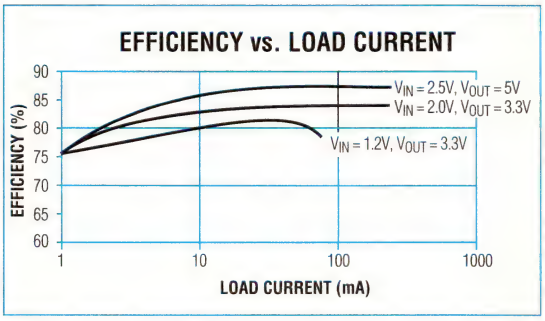


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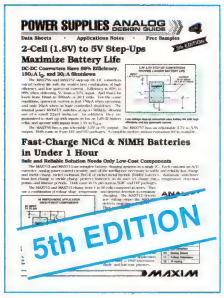


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CIRCLE NO. 79

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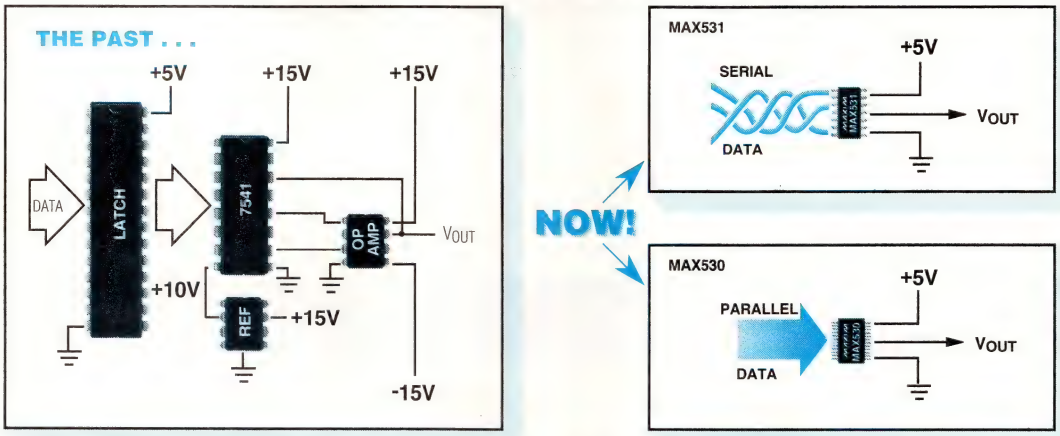


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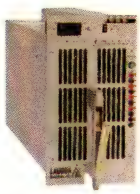
| **PS-31 Series** 10.5"H x 5.6"W x 20"D |  | 1000 Watts | | | |
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CIRCLE NO. 78

# Mainstream applications require optimized assembly language for fast DSPs

John P Sweeney, AT&T Microelectronics

***DSPs are fast, but you have to optimize your code to take advantage of their speed.***

As DSP technology moves away from niches and into mainstream applications for consumer products, designers need to optimize DSP-code efficiency to minimize the power consumption and cost of the end product. Efficient code means you must take advantage of every nuance of your chosen DSP architecture. The examples in this article demonstrate how to use architectural features of the AT&T DSP1600 family to augment the computation-intensive inner loops of table search, filter, and convolutional encoder algorithms.

Optimization of DSP code is key to developing competitive products. Consider emerging digital cellular phones. Most prototypes demonstrated thus far require multiple fixed-point DSPs to perform the digital-cellular algorithms. Efficient coding can eliminate the need for one or more DSPs and result in a lower-cost product that requires less power, both crucial to product success in a cellular-phone market.

Three functions that are useful in a variety of communications-oriented DSP applications such as digital cellular phones include: vector-sum excited linear-prediction (VSELP) codebook search, VSELP 10-pole filter, and forward-error-correction (FEC) convolutional encoder.

You can use VSELP and FEC functions to encode digitized speech. The basic search, filter, and convolutional encoder algorithms are also inherent in many other applications.

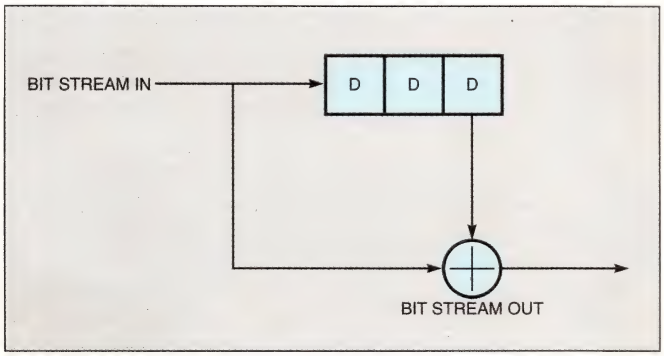


**Fig 1—The convolutional encoder creates an output that is based on a combination of delayed input bits. In this case, it represents the expression $g(D)=1+D^3$.**

A computation-intensive function required in many DSP table and codebook search algorithms is:

$$\max \{A(i)/B(i)\},$$

where i=1, 2 ... N. The exact meaning of parameters A and B aren't important here. Understand, however, that the function requires a search that takes the elements A(i) and B(i) from calculated vectors of size N, and looks for the value of i that maximizes the expression.

In C-like pseudo code you could express the algorithm as:

```
A[best] = 0
B[best] = 1
cnt = 0
for i = 1 ... N {
        if (A[i]/B[i] > A[best]/B[best]) {
                A[best] = A[i]
                B[best] = B[i]
                cnt = i
        }
}
```

It is inefficient to divide when using a DSP. You might want to rewrite the inner loop using an equivalent multiplication operation. You can accomplish this by rearranging the equation to eliminate divisions in favor of multiplications.

```
if (A[i]*B[best] > A[best]*B[i]) {
        A[best] = A[i]
        B[best] =  B[i]
        cnt = i
}
```

The computation-intensive parts of the algorithm are the multiplications and the comparison/selection function. Coding this algorithm efficiently in assembly code requires you to optimize your DSP code, taking advantage of architectural features that can accelerate the signal-coding function. For example, the following assembly-language algorithm for the AT&T DSP1610 or DSP1616 benefits from the conditional "ifc" instructions, which lend themselves to signal-coding applications.

This algorithm assumes RAM precalculates and stores A and B data elements as interleaved entries. The DSP1600 assembly code has a time-stationary C-like syntax. All

instructions on one line execute in parallel in a single cycle, and the results are available for use by instructions on the next line (see **box**, "Reading DSP assembly code").

```
/* Maximize A/B in VSELP codebook search */
/* Input buffer is A[0], B[0], ... A[63], B[63] */

r0 = InputBuffer                    /* r0 points to input*/
pt = InputBuffer                    /* pt points to input*/
c1=-1
c2=-1                               /*set up counters for best pointer*/

a1=a1^a1                            /*clear a1 with XOR*/
                                    /* a1H = initial best A[best] = 0*/
a1=a1+1                             /*a1L = initial best B[best] = 1*/

/* if A[i]*B[best] > B[i]*A[best] then      */
/*                 A[best] = A[i]           */
/*                 B[best] = B[i]           */
/*                 c2 = i                   */
do 64 {
a0=a1<<16                                          /*a0H = B[best] */
                    y=a0        x=*pt++            /*y=B[best] - x=A[i]*/
          p=x*y     y=a1        x=*pt++            /*A[i]*B[best]*/
                                                   /* y=A[best] - x=B[i]*/
a0=p      p=x*y     y=*r0++                        /*B[i]*A[best] - y=A[i]*/
a0=a0-p             yL=*r0++                       /*A[i]*B[best]-A[best]B[i]*/
                                                   /*yL=B[i]*/
ifc pl a1=y                                        /*if A0 flag plus load A1*/
}

/* c2 points to best A and B */
/* No data dependency in this code*/
```

This algorithm benefits from the fact that the DSP1600 family allows both data (Y) and program/coefficient (X) addressing units to access RAM. Traditional DSPs limit program/coefficient access to ROM. The algorithm also takes advantage of the fact that the 36-bit accumulators and the 32-bit y register can store two 16-bit values or a single 32-bit value. For example, a1 initially stores the settings for A[best] in bits 16 to 31 (referred to as a1H for high) and B[best] in bits 0 to 15 (referred to as a1L for low).

Optimizing DSP code requires that you save every cycle by carefully considering each instruction step—even simple ones. For example, The XOR (exclusive or—a1 a1) instructions near the top of this code example set accumulator a1 to 0 without doing an immediate load. DSP1600 family processors can execute the XOR instruction in a single instruction cycle; an immediate load would require two instruction cycles.

The key to this algorithm's efficiency is cross multiplication, which eliminates processing overhead caused by division and the special conditional execution capabilities of the DSP. The DSP's pipelined DAU (data arithmetic unit) performs the calculations efficiently, just as most general-purpose DSPs would. After the comparison, the assembly code executes the equivalent of the pseudo code "if clause" in a single instruction cycle. The quick execution works because the DSP1610/16 instruction,

ifc CON a1=y,

performs the following operations in a single instruction cycle:

```
c1=c1 + 1
if CON {
        c2=c1           a1=y
        }
else    {
        nop
        }
```

CON can be one of any number of tests on the DAU's logical flags. In the code above the instruction "ifc" pl, a1=y (if plus) tests the prior accumulator instruction a0=a0-p for a positive result. A positive result indicates that a new best value has been located. The nop in the pseudo code simply implies that the path length through the code is consistent, regardless of whether the condition passes or fails. Consistent path lengths allow for accurate prediction of worst-case power requirements—a key to commercial DSP implementation.

Another requirement for fast VSELP operation and for most DSP applications is the ability to perform adaptive synthesis filter algorithms efficiently. The following example demonstrates a 10th-order IIR filter implementation. The adaptation is carried out in the lattice-filter domain, but the implementation is applied in direct form. Because of the wide dynamic range of speech and the fixed-point nature of the DSP1600 family some scaling is required during the application of the filter.

This algorithm assumes that buffer r0 points to the feedback-state variable buffer, r1 points to the input-data buffer, r2 points to the output-data buffer, and pointer pt points to the filter coefficients. The basic function of the algorithm is

## READING DSP ASSEMBLY CODE

For the uninitiated, the DSP code in this article can appear rather cryptic, but the code is actually easy to read once you realize that the structure is analogous to the structure of a DSP. The AT&T DSP1600 family of processors and most other DSPs have four key pipelined elements: an X memory addressing unit typically used to access ROM, a Y memory addressing unit typically used to access RAM, a multiplier, and an ALU. The hallmark of DSPs is their ability to fetch two operands and perform a multiply and an accumulate in a single instruction cycle.

The structure of the DSP assembly code exactly matches the DSP architecture. A single line of code can include four operations. The code is called "time stationary" because all four instructions on a line execute simultaneously. The left-most instruction column includes only instructions relative to the ALU. The second column from the left includes multiplication instructions, and the third and fourth columns from the left are used to load the Y and X operands, respectively. The Y addressing unit has four dedicated pointers (r0, r1, r2, and r3) because you typically use it to access RAM. The X unit has a single dedicated pointer (pt).

The DSP1600 family processors also have three dedicated counters (c0, c1, and c2), two accumulators (a0 and a1) with alternate accumulators (aa0 and aa1), and three auxiliary BMU (bit-manipulation unit) registers (ar0, ar1, and ar2).

While all instructions on a single line execute in parallel in a single instruction cycle, the data flow is in different stages of the processor pipeline. Operands loaded into the X and Y registers in one line would multiply in a subsequent line, and the result would accumulate in a third line. The programmer controls the data flow through the pipeline.

to perform the dot product of the feedback states and the filter coefficients by multiplying each state/coefficient pair and summing the results.

```
                    /* VSELP 10 pole synthesis filter */

r1=InputData                    /*input data stream pointer*/
r2=OutputData                   /*output data stream pointer*/
r0=StateBuffer          /*feedback variable buffer*/
rb=StateBuffer          /*cyclic addressing around feedback*/
re=StateBuffer + 9              /*variables buffer of 10 words*/
pt=Coefficients                 /*10 denominator coefficients*/
i=-9                            /*Coefficient pointer reset value*/
ar0=N                           /*set scaling constant*/

/*first pass of filter*/
a0=p                    y=*r0++     x=*pt++     /*start pipeline*/
a0=a0-p     p=x*y       y=*r0++     x=*pt++     /*calc states*coeffs*/
do 7{
a0=a0+p     p=x*y       y=*r0++     x=*pt++
}
a0=a0+p     p=x*y       y=*r0++     x=*pt++i    /*reset pt*/
a0=a0+p     p=x*y                               /*flush pipeline*/
a0=a0+p                 y=*r1++                 /*get input data*/
a0=a0<<ar0                                      /*scale denominator*/
a1=a0+y                                         /*add input*/
a1=rnd(a1)                                      /*round result*/
```

The first pass of the filter calculates an initial value for the feedback state and stores the value in accumulator a1. By segmenting the code into first-pass and main-filter loops, you also ensure that the main part of the filter routine will fit into the instruction cache on the DSP1610/16, thereby speeding the repetitive multiply/accumulate process.

The first pass also demonstrates another way that you can code even simple instructions to save DSP cycles. The first two accumulator instructions, a0=p and a0=a0-p, actually serve to set accumulator a0=0. An explicit a0=0 instruction would have required two dedicated instruction cycles to perform the immediate load operation. Even an XOR operation requires one dedicated instruction cycle because the instruction can't execute concurrently with pipeline load instructions. The initialization is essentially performed for free (with no instruction cycle overhead). The first two accumulator instructions execute in parallel with the two instructions necessary to load the pipeline before performing the do loop.

This algorithm processes 40 data words in a VSELP speech coder.

```
                /*main part of filter -- single cycle RAM*RAM multiply accumulates*/
do 39{
                                y=a1        x=*pt++     /*y=latest output*/
                p=x*y           y=*r0++     x=*pt++     /*start pipeline*/
    a0=p        p=x*y           y=*r0++     x=*pt++
    a0=a0+p     p=x*y           y=*r0++     x=*pt++     /*states x coeffs*/
    a0=a0+p     p=x*y           y=*r0++     x=*pt++
    a0=a0+p     p=x*y           y=*r0++     x=*pt++
    a0=a0+p     p=x*y           y=*r0++     x=*pt++     /*a0 sums dot product*/
    a0=a0+p     p=x*y           y=*r0++     x=*pt++
    a0=a0+p     p=x*y           y=*r0++     x=*pt++
    a0=a0+p     p=x*y           y=*r0++     x=*pt++i    /*reset pt*/
    a0=a0+p     p=x*y           *r2++=a1                /*write output*/
    a0=a0+p                     y=*r1++                 /*read next input*/
    a0=a0<<ar0                                          /*scale denominator*/
    a1=a0+y                     *r0=a1                  /*store output again*/
    a1=rnd(a1)                                          /*form next output*/
    }
    *r2++=a1                        /*write last output*/
    *r0--
    *r0=a1                          /*write last state update*/
```

Note the following features of the filter algorithm. Cyclic addressing is applied to the Y-space memory accesses. The DSP1600 allows you to define a buffer that is pointed to by r0, r1, r2, or r3 (four pointers that are dedicated to the Y memory space) and bounded by rb and re. In this case, registers rb and re define a 10-word cyclic buffer. The DSP1600 performs the pointer-reset operation with no instruction-cycle overhead. The X memory fetches operate in another RAM buffer, and the reset of the X pointer is reset explicitly using the post modification of the pt register by i.

The efficiency of this filter algorithm comes as a result of the code's use of the instruction cache integrated on the DSP1610 and DSP1616 processors. You can use the DSP1600 "do" operation to explicitly load the instruction cache. The cache holds the repeating section of the filter routine that computes the dot product. The instructions execute in two cycles the first time through the loop. Subsequent iterations of the filter don't require an instruction fetch from memory, and, therefore, execute in a single instruction cycle.

The algorithm works properly because the coefficient fetches from the X memory space are fetches from the internal RAM of the DSP. The internal RAM is dual-ported and accessible by both X and Y addressing units. Therefore, the adaptive coefficients can be read by the X space and written by the Y space. Each loop iteration performs an arbitrary scaling of the denominator before final output rounding. The two accumulators implement a delayed-feedback pipeline to minimize instruction cycles and memory accesses. The first pass of the filter sets up the delayed feedback by loading a1 with an initial state, and each pass through the main routine also passes a value for a1 back to the beginning of the loop.

You may notice that the main part of the filter loop includes the following line:

```
a0=a0+p p=x*y y=*r0++ x=*pt++
```

This line is repeated exactly seven times. The code for the first part of the filter used a do construct to simplify these load/multiply/accumulate lines and to take advantage of the instruction cache. The main part of the filter, however, needs the instruction cache to be loaded with instructions that speed iterations of the main loop. Adding a looping construct with a conditional "if" statement would reduce the number of lines of code and would also add instruction-cycle overhead. Explicitly repeating the seven lines ensures single cycle execution due to the use of the instruction cache.

Another computation-intensive algorithm found in many DSP applications is convolution. Convolutional encoders, for example, are used to add structure and redundancy to bit streams that need to be transmitted via a medium that isn't guaranteed error-free. The structure that convolution adds, FEC, allows errors to be corrected at the receiver.

A convolutional encoder uses a generating equation that expresses output bits as a combination of delayed input bits. The amount of delay is specified by an exponential power of the unit-delay operator D. You can combine the bits using an XOR function. For example, consider the expression:

$$g(D)=1 + D^3.$$

The diagram in **Fig 1** represents this generating expression. The output bit depends only on previous inputs and not

## OPTIMIZING DSP CODE

on previous outputs. Thus, the encoder has a finite impulse response. The maximum delay (the current element plus the total number of delay elements) in the generating polynomial is called the "constraint length" of the encoder. For example, an encoder with a constraint length of six has a maximum of five delay elements and 32 discrete states that it can assume.

The delay elements are essentially single-bit latches. The group of three delays in **Fig 1** can be thought of as a 3-bit shift register. The content of the 3 bits at any time constitutes a discrete encoder state out of eight possible discrete states. The algorithm below implements the $1+D^3$ encoder described in the example above:

```
a0=*r0--          /*get the last 16 bits*/
a0L=*r0           /*get previous 16 bits*/
a0=a0<<4          /*shift left 4 bits into guard bits*/
a1=a0<<3          /*form the D^3 term*/
a0=a0^a1          /*XOR to place 16 bits of 1+D^3 in a0*/
```

The algorithm reads 16-bit words one at a time from the end of a bit-stream buffer. The loaded accumulator is left-shifted by 4 bits into the accumulator guard bits. By shifting the input word into guard bits, the algorithm ensures that the most-significant accumulator bit is not affected by the sign bit during later accumulator operations. The accumulator can be restored after the XOR operation. The delayed bits form in a1 by left-shifting a0 by 3 bits, representing the input-bit stream delayed by 3 bits. The XOR operation generates a 16-bit word that represents 16 bits of the bit stream processed by the polynomial.

Note that the algorithm reads two 16-bit words into accumulator a0 yet generates only a single 16-bit output. The second 16-bit input word is required to generate the proper output bits for the 3 least-significant bits of the first 16-bit word.

Advanced signal coders for applications such as digital cellular use two or more polynomials with several delay elements. A first polynomial adds structure to the bit stream, and a second polynomial adds redundancy. The two polynomials generate 2 output bits (called a di-bit) for each input bit. This is known as a rate ½ convolutional encoder.

You can implement such a convolutional encoder using an efficient parallel algorithm that encodes 16 bits in a single pass. To optimize the implementation, you must store the input-bit stream in discrete 16-bit words and feed it efficiently into the generating equations. The key to efficient implementation is a DSP architecture that includes barrel-shift capabilities and an instruction set that supports arbitrary shift distances.

A convolutional encoder for North American digital cellular creates the two output words using the equations specified by the following expressions:

$$g0(D) = 1 + D + D^3 + D^5$$

$$g1(D) = 1 + D^2 + D^3 + D^4 + D^5.$$

An efficient way to implement this algorithm is to calculate g0(D) and then calculate g1(D) using the following expression:

$$g1(D) = g0(D) + D + D^2 + D^4.$$

The XOR operation used to sum bits allows the dual occurrence of the D term to cancel each other thus properly removing the D term from the g1(D) expression.

The following algorithm implements an encoder for the above equations:

```
                /*FEC Convolutional Encoder*/
                /*using rate 1/2 convolutional encoder*/

Convcode:
                c0=1-6                  /*loop for 6 data words*/
```

Note that counter c0 is set to -5 but is expressed as 1-6 for readability; this example makes six passes through the loop starting at ConvLoop. Six passes are necessary to encode each speech segment in a North American digital cellular phone.

Also note that c0 is never explicitly incremented because the DSP1600 "if c0" statement found later in the code automatically increments the counter.

```
ar1=1                   /*shift distance of 1*/
ar2=2                   /*shift distance of 2*/
ar0=4                   /*shift distance of 4*/
```

Registers ar0, ar1, and ar2 are auxiliary BMU registers. Using these registers to store shift distances allows the actual shift instructions to execute in a single instruction cycle. A shift instruction that uses immediate operands such as 1, 2, and 4 would require two instruction cycles.

```
ConvLoop:
        a0=*r0--            /*fetch low 16 bits to encode*/
        a0L=*r0             /*fetch higher 16 bits*/
        a0=a0<<ar0          /*move data into guard bits*/
        a1=a0:aa0           /*store D0 in aa0, junk a1*/
```

The instruction a1=a0:aa0 performs three operations. The instruction swaps the contents of accumulator a0 with the contents of alternate accumulator aa0. The instruction stores the value that was originally in aa0 in a1, although that isn't important here because a1 is reassigned in the next instruction, and the instruction sets the DAU logical flags based on the value moved into a1.

```
Calc_g0:
        a1=a0<<ar1          /*a1=D1*/
        a0=a0^a1            /*a0=D0+D1*/
        a1=a1<<ar2          /*a1=D3*/
        a0=a0^a1            /*a0=D0+D1+D3*/
        a1=a1<<ar2          /*a1=D5*/
        a0=a0^a1            /*a0=D0+D1+D3+D5=g0*/
        a0=a0>>4            /*shift g0 out of guard bits & sign*/
        a1=a0:aa0           /*save signed g0 in aa0, a1=D0*/
        a0=a0<<ar0          /*g0 back into guard bits*/
Calc_g1:
        a1=a1<<ar1          /*a1=D1*/
        a0=a0^a1            /*a0=D0+D3+D5*/
        a1=a1<<ar1          /*a1=D2*/
        a0=a0^a1            /*a0=D0+D2+D3+D5*/
        a1=a1<<ar2          /*a1=D4*/
        a0=a0^a1            /*a0=D0+D2+D3+D4+D5=g1*/
        a0=a0>>4            /*shift g1 out of guard bits & sign*/
```

Calculating g0 and g1 is straightforward, provided that the DSP can efficiently handle arbitrary shifts . The above algorithm generates the delayed terms by left-shifting the 32 bits

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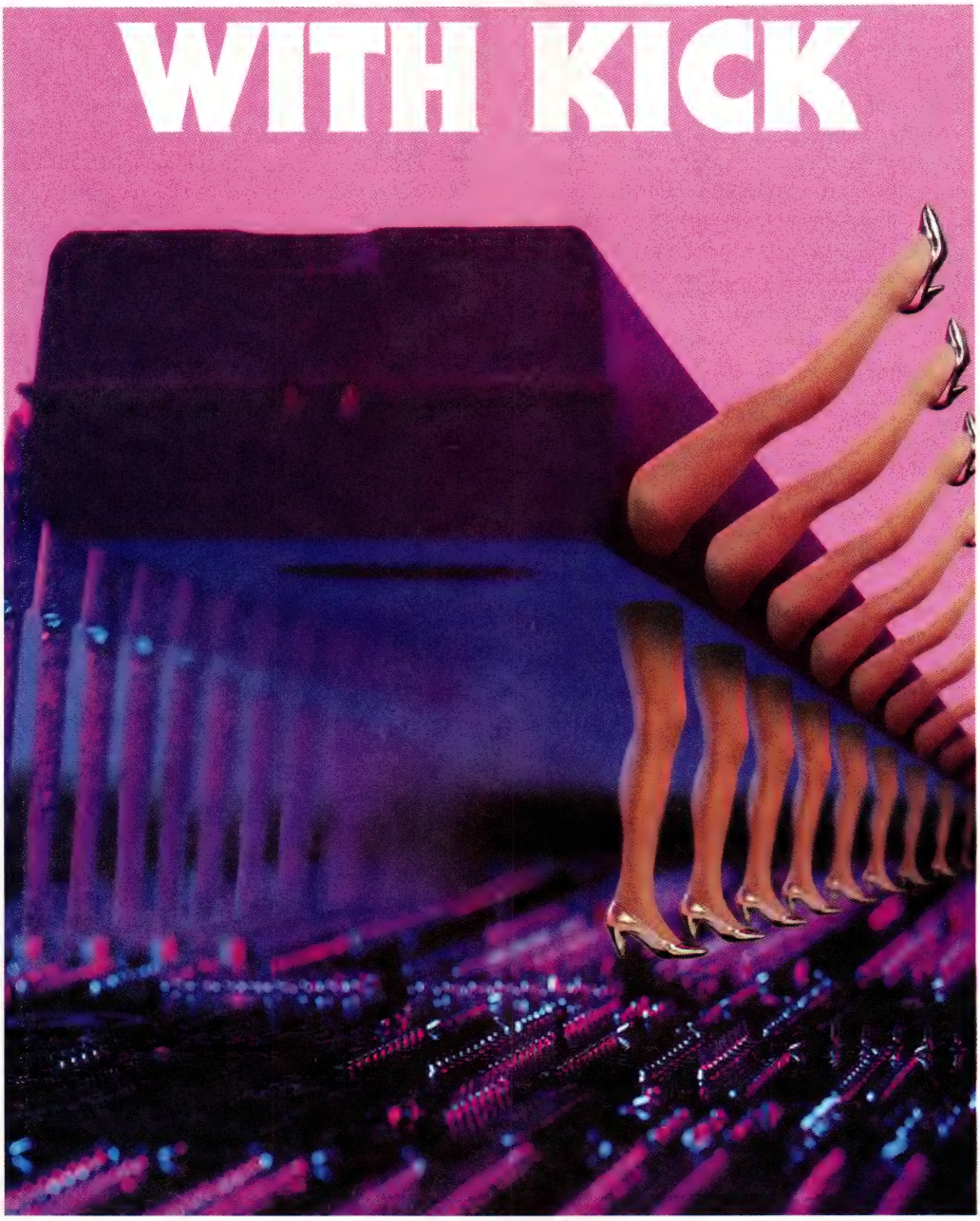

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## OPTIMIZING DSP CODE

of data in a1. Delayed terms are accumulated using XOR operations on a0. At this point in the code, alternate accumulator aa0 holds g0 and accumulator a0 holds g1.

Almost any encoding application, however, requires that the di-bits are interleaved for transmission. The following DSP1610/16 code performs the interleave operation, taking advantage of the instruction cache and the ability to swap the contents of aa0 and a0 in a single instruction cycle, eliminating the overhead that traditional DSPs would encounter due to dedicated data-load instructions.

```
Interleave g0g1:
        do 32{
        a1=a1<<1            /*make room for next bit in a1*/
        a0=a0:aa0           /*swap g0 & g1, set sign bit*/
        if mi a1=a1+1       /*store sign bit in lsb of a1*/
        a0=a0<<1            /*shift out tested bit*/
        }
        *r1--=a1            /*store 16 interleaved bits*/
        *r1--=a1            /*store next 16 interleaved bits*/
        if c0 lt goto ConvLoop  /*c0 is tested and incremented*/
```

The left shift of a1 makes room for each succeeding bit of the interleaved result. The next instruction swaps g0 and g1 between a0 and aa0 and sets the DAU flags based on the new contents of a0. The "if minus" instruction essentially tests the most-significant bit of a0 from the previous instruction and adds 1 to a1, which holds the result, if the most-significant bit in a0 is a 1. By adding 1 to a1, the instruction sets the least significant bit in a1 to a 1. The final left-shift of a0 prepares the current contents of a0 to test the next bit two iterations of the loop later (because of the swap of a0 and aa0). After 32 iterations of the loop, the 16-bit values that g0 and g1 represent have been interleaved, and the resulting 32 bits have been stored in a buffer pointed to by r1.

Once the instruction-cache do loop completes the interleave for one 16-bit input, the "if c0" instruction tests to see if the counter has reached 0. The instruction automatically increments c0 after each test, so that, after the sixth time through the loop, the test fails, and processing is done. EDN

### Author's biography

*John P Sweeney is a senior applications engineer with AT&T Microelectronics, where he provides support for system hardware and software used in digital-cellular applications. He holds a BSEE degree from Villanova University, Villanova, PA, and in his spare time enjoys music, high-fidelity equipment, racquetball, tennis, and golf.*

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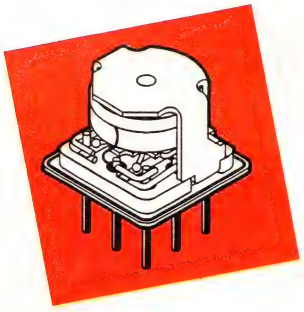

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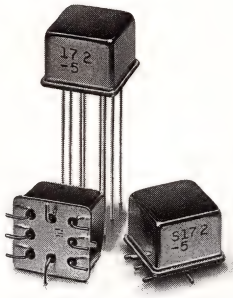


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CIRCLE NO. 109

# A transaction approach to error handling

Bruce A Rafnel, Hewlett-Packard Co

***You can apply the transaction-based recovery concept used in databases to any application. Doing so helps provide more reusable and maintainable programs.***

Programs contain two major paths: a forward path that does the work and a reverse path that rolls back the work when the program detects errors. Typically, these paths are so tightly bound together that both paths are difficult to read. Code that is difficult to read results in code that is difficult to write, debug, enhance, and reuse.

For example, in object-oriented programming, you cannot reuse objects as much as you might want, primarily because the objects are tightly bound together at the error-handling level. Many times, error code even gives clues about how a program implements an object.

The solution is to handle errors in programs as you would in a database-transaction recovery mechanism. A database transaction is a unit of work that involves one or more operations on a database. For example, the operation of inserting data into a database could be a transaction if it's the only operation performed. If you combine the insertion with an update, the program considers both operations as one transaction. In a database transaction, the transaction either executes in its entirety, or, if an error appears in any of its operations, the transaction totally cancels as if it had never executed. If an error appears, the program automatically rolls back all work to the beginning of the transaction.

When a development team first introduces transaction error handling to a project, many engineers resist it because it requires the removal of IF statements after calls to functions. Engineers also believe the technique makes debugging more difficult. However, after seeing how much easier it is to read and write transaction error-handling code, the resistance fades. In addition, transaction error handling decreases debugging time to a little less than that of the traditional method. The reason for this decrease is probably that transaction error handling has less embedded error-handling code, causing defects to stand out more. Also, when you add error-handling code, you do so in the structured way that most engineers like to work—a method that disturbs very little of an already-debugged program.


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Software developers are often dismayed at how difficult commercial programs are to maintain and design, compared with programs they developed in school. The reason for this may be that the programs students develop in school are "toys" that assume perfect inputs and that the hardware has unlimited memory and disk space. In addition, most software engineers have very little formal training in error-handling methods. Typically, software developers learn error handling by example or by trial and error, and they use the traditional error-handling model: Check for an error, find an error, and return an error code.

Many formal design processes, such as structured analysis and structured design, recommend that developers ignore errors during design because such errors are an implementation detail. However, this "minor" detail can take up to one-third of the code in commercial programs. This code appears not just around algorithms but directly in the middle of the algorithms. The resulting programs are difficult to read, debug, and reuse.

In addition to existing design methodologies, such as structured analysis and structured design, is exception handling, or error handling. This programming style separates most of the error-handling processes from the main algorithms. Error handling comprises four main parts: detection,

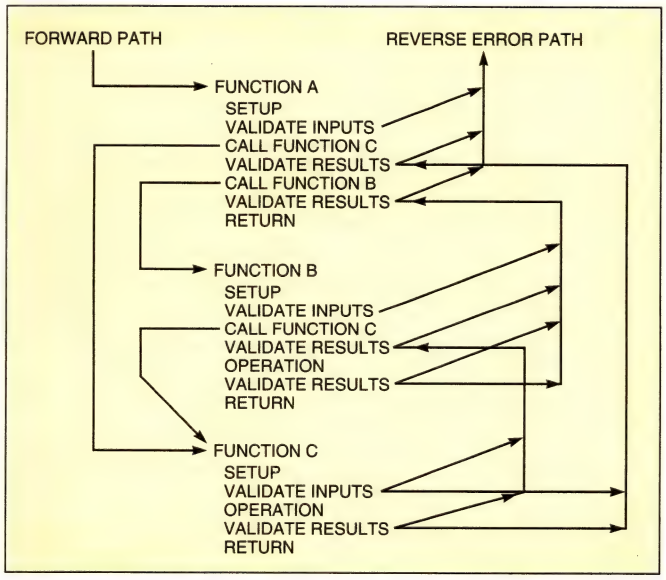


**Fig 1—In traditional error-handling program flow, the forward path does the work of the program, and the reverse path does the error handling. Error-handling code appears throughout the algorithm.**

correction, recovery, and reporting. The main focus of this article is error recovery.

In this context, the term "error" does not refer to a defect but to an exception that an algorithm cannot handle. A "defect," on the other hand, is an error that strains the design limits of an entire application or a system. For example, many algorithms assume that there is unlimited memory. Insufficient memory for the algorithm to complete successfully constitutes an error, and you must design the whole application to handle these out-of-memory errors. A defect occurs when an application that does not handle these errors causes a program to halt or to behave in an undocumented way. In other words, whether something is an error or a defect depends on what level of the software hierarchy you are observing.

**Mixed forward and reverse path problem**

**Fig 1** shows the two major paths in commercial programs. The forward path does the work for which a program is designed. The reverse path is the error-handling code that keeps the forward path working correctly. It does this by detecting and fixing problems and rolling back partially completed work to a point at which the algorithm can again continue forward.

An intermediate function in a program has to stop what it is doing in the middle of the algorithm because the program called a function that cannot complete its task. This can lead to "tramp errors," a term similar to the "tramp-data" term of structured analysis and structured design (**Ref 1**).

Tramp errors in functions do not directly relate to the current function but are the result of a real error occurring in a lower-level function. For example, *function A()* calls *function B()*. *Function B()* needs some memory, so it calls the *malloc()* memory-allocation function. The *malloc()* function returns an out-of-memory error. This is a real error for the *malloc()* function. *Function B()* does not know how to get more memory, so it has to stop and pass the error back to *function A()*.

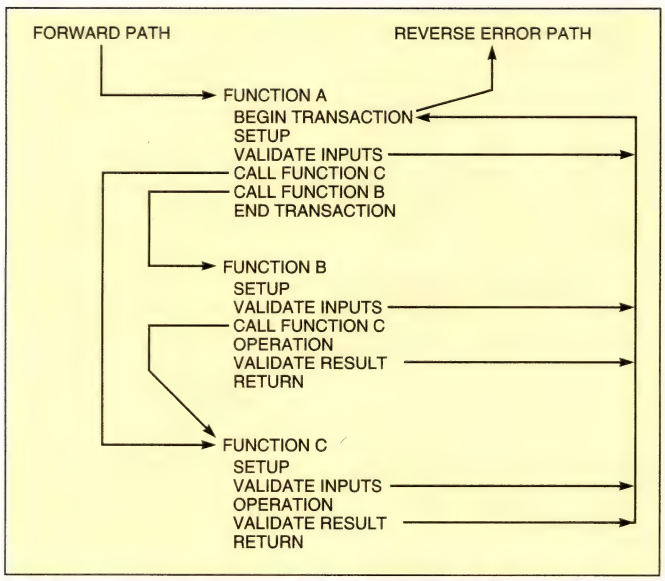


**Fig 2—In transaction error-handling program flow, only error-detection code for real errors remains, and most of the error-correction and recovery code clusters around the beginning and end of the transactions.**

From the perspective of *function B()* and probably *function A()*, an out-of-memory error is a tramp error.

Tramp errors prevent functions from becoming "black boxes." For example, *function A()* (above) now knows something about how *function B()* works. In other words, tramp errors form a part of error recovery—not error detection—because if the program could immediately correct real errors, tramp errors would not occur. Because of tramp errors, almost every function has to handle errors that lower-level functions generate. This buck-passing can cause tight data coupling, which makes code reuse more difficult.

**Unreadable code and poor reuse**

Mixed forward and reverse paths and tramp errors combine to obscure the main forward path of the program, which is doing the real work. The correction and recovery parts of error handling are the main areas that obscure the code. Most of the code for detection and reporting can be in separate functions, so these components of error handling play less of a role in obscuring code than do the other two.

You can solve the problems of unreadable code and poor reuse by separating the forward and reverse error-processing paths and by using context-independent error codes. This method of error handling is very similar to the way databases handle error recovery. Transactions control the rollback process when a group of database operations cannot complete successfully.

The traditional defensive way of programming is to assume that a function may have failed to complete its task, resulting in a lot of error-handling code to check for the errors and to roll back partially completed work, as **Fig 1** shows. Now, assume the reverse—that returning functions have successfully completed their tasks. In this scenario, if the function or one of the functions it calls has errors, the function passes processing control to a programmer-defined recovery point. In other words, the programmer defines transaction points so that if there are any problems, the work rolls back to those points, and the processing again proceeds. With this approach, you do not need to check for errors after each function call, and tramp error-detection code does not clutter the forward path.

Context-independent error codes provide more information than just an error number. They also provide information such as which function generated an error, the state that caused the error, the recommended correction, and the error severity. This information allows the program to correct the error in a location separate from the forward processing path.

Programmers usually encode contexts of errors for error-reporting functions. For example, error contexts may include the names of the program, the function, the error type, and the error code. The program saves these parameters to report later. However, programmers rarely use sophisticated encoding schemes because traditional error handling already knows the context of the error: Checking occurs right after a call to the offending function.

With transaction error handling, the recovery process is separate from the forward processing path, necessitating the use of context-independent error codes. This may involve creating unique error codes across a whole application or system (with the codes bound at compile time). An alternative

would be to assign code ranges or other unique identifiers to functions at runtime.

**Code readability and reuse**

The transaction error-handling approach makes programs easier to read because the reverse-processing paths are visually separate from the forward-processing paths. This method makes possible creating some general error-recovery interfaces so that functions (modules or objects) connect only loosely at the error-handling level. This loose connection is possible because the there are fewer tramp errors to control the recovery process, and the program needs to handle only the real errors.

Two methods you need for building a transaction error-handling library are transaction-control and transaction-data management. Transaction-control management requires some language support to implement the mechanism that controls error recovery. For example, languages like Hewlett-Packard Co's Pascal-MODCAL have a "try/recover" feature that can support a transaction error-handling style.

For other languages, you must use a "global-goto," or "multithreaded," feature, which allows a lower-level function and all other functions above it to exit to a point you define in a higher-level function without passing error-code flags through all the other functions. In C, you do this with the *setjmp* and *longjmp* library routines. The *setjmp* function saves its environment stack, and *longjmp* restores that environment. The **listings**, which are written in C, show how these functions work.

The material in **Ref 2** details the new C++ exception-handling feature, which provides an excellent foundation for a transaction-based error handler. The material in **Ref 3** also describes how to add C++ error-handling functions to regular C programs. However, overuse of transaction error handling can lead to code that is just as cluttered as the traditional error-handling style. You must design transaction boundaries for objects with the same care that you would to design an object's interface.

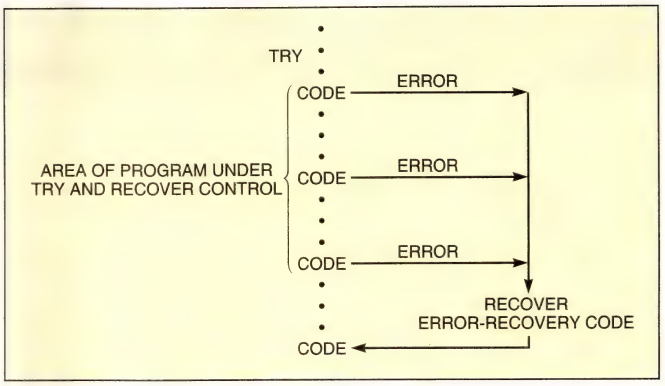


**Fig 3—A try/recover statement defines error-recovery code that executes if a program detects an execution error within a particular area.**

If a language is missing a global-goto or multithreaded feature, use macros or other "wrapper" functions to build recovery processes that are mostly invisible. Wrapper functions and macros add functionality to functions that you cannot change, such as library functions.

In building a transaction-handling package, you might want to give it the following features:

- Allow nested transactions by keeping the transactions' beginning points on a stack.
- Allow functions to share a common transaction stack.

## LISTING 1 - TRADITIONAL ERROR-HANDLING STYLE

```
/*   read.c - Read a binary formatted file                          */
/*   This program reads and prints a binary file that has the       */
/* following structure:                                             */
/*                                                                  */
/*   Record type code (The last record has a value of 0)            */
/*   Size  Number of characters in Msg                              */
/*   Msg   0 to 2048 characters                                     */
/*   Record type code                                               */
/*   Size                                                           */
/*   Msg                                                            */
/*   .                                                              */
/*   .                                                              */
/*   .                                                              */

#define aExitErr(pMsg, pErr)      puts(pMsg); exit(pErr)
#define aRetErr(pMsg, pErr)       puts(pMsg); return(pErr)

typedef struct {
     long   Type;
     int    Size;
}    aFileHead;
/*                                                                  */
/*   Forward Algorithm:                                             */
/*                                                                  */
/*   Main                                                           */
/*      1. Open the file.                                           */
/*      2. Call the Read process.                                   */
/*      3. Close the file.                                          */
/*                                                                  */
main() {
     int     Err;
     FILE *  InFile;
     if ((InFile = fopen("file.bin", "rb")) == NULL) {
               aExitErr("Error: Could not open: file.bin",1);
     }
     if ((Err = aRead(InFile)) != 0) {
               aExitErr("Error: While reading: file.bin", 2);
     }
     if (fclose(InFile) {
               aExitErr("Error: Closing: file.bin", 9);
     }
}/* main() */

/*   Forward Algorithm continued:                                   */
/*                                                                  */
/*   Read Process                                                   */
/*   1. Read the Type and Size values.                              */
/*   2. If Type = 0, exit.                                          */
/*   3. Read Size number of characters into the                     */
/*      Msg variable.                                               */
/*   4. Print the Msg.                                              */
/*   5. Go to step 1.                                               */
/*                                                                  */
int aRead(pHandle)
     FILE *  pHandle;
{
     int                 Err, N;
     char *              Msg;
     long                RecNum;
     aFileHead           RecHead;

     if ((Msg = (char *) malloc(2048)) == NULL) {
               aRetErr("Error: Out of memory", 3);
     }
     RecNum = 0L;
     while (1) {
          if (fseek(pHandle, RecNum, SEEK_SET) < 0) {
                    aRetErr("Error: in fseek", 4);
          }
          N = fread((char *) &RecHead, sizeof(aFileHead), 1, pHandle);
          if (N < 0) {
                    aRetErr("Error: in fread", 5);
          } else if (N != 1) {
                    aRetErr("Error: short fread", 6);
          }
          if (RecHead.Type == 0L) {
                    return(0);          /* EOF */
          }
          if (RecHead.Size) {
                    if ((N = fread(Msg, RecHead.Size, 1,
                         pHandle)) < 0) {
                              aRetErr("Error: in fread", 7);
                    } else if (N != 1) {
                              aRetErr("Error: short fread",8);
                    }
                    if ((Err = aPrint(Msg,
                         RecHead.Size)) != 0) {
                              aRetErr("Error: in aPrint", Err);
                    }
          }
          RecNum = RecNum + RecHead.Size + sizeof(aFileHead);
          }
} /* aRead() */
```

## LISTING 2 - TRANSACTION ERROR-HANDLING METHOD

```
/*   read.c - Read a binary formatted file                          */
/*   This program reads and prints a binary file that has the       */
/*   following structure:                                           */
/*                                                                  */
/*   Record type code (The last record has a value of 0)            */
/*   SizeNumber of characters in Msg                                */
/*   Msg  0 to 2048 characters                                      */
/*   Record type code                                               */
/*   Size                                                           */
/*   Msg                                                            */
/*                                                                  */
#include"erpub.h"
#include"epub.h"
typedef struct {
     long  Type;
     int   Size;
} aFileHead;
/*                                                                  */
/*   Forward Algorithm:                                             */
/*                                                                  */
/*   Main                                                           */
/*      1. Open the file.                                           */
/*      2. Call the Read process.                                   */
/*      3. Close the file.                                          */
/*                                                                  */
main() {
     FILE *  InFile;
     erRecOn = 1;
     if (erSet()) { /* Transaction rollback point */
        printf("Error: %d in function: %s\n", erErr,
                erFun);
        erUnset();
        exit(1);
     } /* End Recovery section */

     InFile = fopen("file.bin", "rb");
     aRead(InFile);
     fclose(InFile);
     erUnset();
} /* main() */
/*   Forward Algorithm continued:                                   */
/*                                                                  */
/*   Read Process*/                                                 /*
/*      1. Read the Type and Size values.                           */
/*      2. If Type = 0, exit.                                       */
/*      3. Read Size number of characters into the                  */
/*         Msg variable.                                            */
/*      4. Print the Msg.                                           */
/*      5. Go to step 1.                                            */
/*                                                                  */
int aRead(pHandle)
     FILE * pHandle;
{
     char *    Msg;
     long      RecNum;
     aFileHead RecHead;
     Msg = (char *) malloc(caMsgLen);

     RecNum = 0L;
     while (1) {
          fseek(pHandle, RecNum, SEEK_SET);
          fread((char *) &RecHead, sizeof(aFileHead), 1, pHandle);
          if (RecHead.Type == 0L) {
               return;/* EOF */
          }
          if (RecHead.Size) {
               fread(Msg, RecHead.Size, 1,pHandle);
               aPrint(Msg, RecHead.Size);
          }
          RecNum = RecNum + RecHead.Size + sizeof(aFileHead);
     }
     } /* aRead() */
```

- Allow functions to define their own transactions with a common transaction stack, or allow functions to define their own transaction stacks for special cases.
- Define special transaction points to handle errors in common categories. (For example, abort the whole program, restart the whole program, close all files and restart, close current file and restart, and release all memory not needed and restart.)
- Have the transaction error handling turn on and off. (When transaction error handling is off, a function returns error codes in the traditional way.)
- Define expected errors for some functions by masking out the needed errors. (You can simulate this feature by turning off transaction error handling, but then you also have to manage unexpected errors.)

### Transaction-data management

Recovery involves more than just rolling back functions to undo some intermediate work. It may also involve releasing unneeded memory or changing global variables back to the values they had at the beginning of the transaction.

You can best manage memory using a mechanism similar to the mark/release memory feature in some implementations of Pascal. The mark/release procedures allow dynamic allocation and deallocation of memory in an executing Pascal program. The C functions *malloc()* and *free()*, along with a stack of pointers to track the allocated memory, provide the best features for allocating and freeing memory. With these features, you can call a mark function just before the program's transaction starting point to mark the current stack point. If a *longjmp()* goes to this recovery point, the release function is called to free any memory allocated after the mark point.

To remove pointers from the mark/release stack, you need a commit function at the end of a program transaction. The commit function indicates the successful completion of a transaction in the database context. You must also consider nested transactions, however. A simple solution would be to have each transaction keep its own mark/release stack.

## LISTING 3 - MACROS AND GLOBAL DATA STRUCTURES

```
     /* erpub.h - Error Recovery Public Include file */
     #include<setjmp.h>
     /* Private Variables */
     #define vMaxEnv       5
     jmp_buf vEnv[vMaxEnv];
     int
vLevel = -1;
     /* Public Variables */
     #define cerFunNameLen 32
     #define erSet()      setjmp(vEnv[++vLevel])
     #define erUnset()    - -vLevel
     #define erRollBack(pFun, pErr, pRet)  \
             strncpy(erFun, pFun, cerFunNameLen); \
             erFun[cerFunNameLen-1] = \0;\
             erErr = pErr;\
             if (erRecOn && vLevel >= 0) { \
                  longjmp(vEnv[vLevel], pErr);\
             } else { \
                  return(pRet);\
     } int   erErr = 0;
     char    erFun[cerFunNameLen];
     int     erRecOn = 0;
```

You can roll back global and other static variables with a strategy similar to the one in the memory-management problem. Just before a transaction's beginning point, the program saves on a stack the states of all the globals that might change. This strategy allows you to nest transactions.

### Context-independent error codes

The traditional error-handling style of checking error codes after each function call automatically gives errors a context. The transaction error-handling style provides this context information in another way. The biggest challenge in transaction error handling is that error codes alone are not very useful. For example, "97" could be the letter "a" in ASCII code, the digits "6" and "1" in BCD format, index 97 in a message array, the 97th error, an out-of-memory error, a disk-full error, a divide-by-zero error, or another error.

To decode an error code, a program must know the source of the error. Some information that the program may save when an error occurs includes the machine name, the program name,

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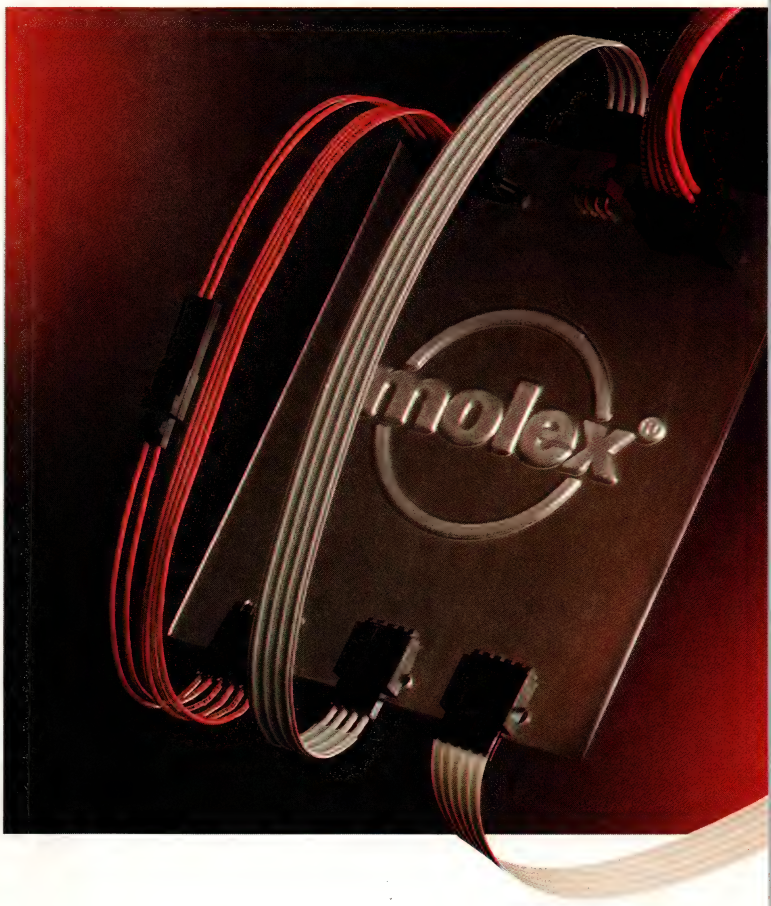


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the process number, the module name, the function name, and, of course, the error code. The program needs to send this information only when it must roll back a transaction.

The amount of information that the program saves depends on the location of the transaction-recovery point and on the runtime environment. For example, a client-server application may need more information than does a simple PC application. Each recovery point can usually find higher-level context information fairly easily. For example, the names of the machine, program, module, and function can easily pass down to a lower-level recovery point. However, a program cannot collect lower-level context information because, by the time the program gets down to that level, the function that had the error would no longer be active.

You may want to consider the following points when implementing a transaction error-handling scheme:

- Put the rollback points, if any, at the beginning of functions.
- Put error detection and default substitution at the beginning of functions.
- Put some error-detection code in the middle of functions to check intermediate values.
- Put error-detection code at the end of functions to validate the results.
- Do not put error-handling code for managing rollbacks in the middle of a function.

**Traditional error-handling style**

**Listing 1**, which reads a binary formatted file, is coded with a common error-handling style. The code would have been more cluttered without the *aExitErr()* and *aRetErr()* macros to manage the error reporting and recovery. **Listing 1** uses the simple error-recovery process: Detect error, report error, and exit. However, notice how much error-handling code is mixed in with the algorithm.

**Listings 2** through **5** show an implementation of the transaction error-handling style. **Listing 2** performs the same function as the program in **Listing 1** but uses the transaction style of error handling. The functions *erSet*, *erUnset*, and *erRollBack* provide the error handling defined in the include file *erpub.h*. **Listings 3** through **5** show the support functions for the transaction error-handling method. In the main body of the algorithm, the code following the recovery sections is clearer than that in the traditional error-handling example, and there is no error-handling or recovery code mixed in with the algorithm.

However, there are some shortcomings in the support modules. For example, most of the macros should be functions, and the program should save the *vEnv* values in a linked list. Some engineers point out that the transaction implementation of *read.c* is not really shorter than the traditional implementation of *read.c* because the error-handling code simply moves from *read.c* into the support functions. But that is exactly the goal: to remove the error-handling code from most functions and encapsulate the error-handling in common shared code.

The include file *epub.h* contains wrapper macros that cause the program to call the appropriate transaction error-handling functions instead of the standard library function. For example, when invoking the standard function *fclose*, the program actually calls the function *eClose*.

**Listing 3** defines macros and global data structures that form a crude error-transaction manager. The macros perform the following operations:

- **erSet**. This macro adds a rollback point to the *vEnv* (environment) stack.
- **erUnset**. This macro removes the top rollback point from the *vEnv* stack.
- **erRollBack**. This macro saves the function name and error code in a global area (*erFun* and *erErr*), and if the *erRecOn* flag is true, control passes to the rollback point defined on the top of the *vEnv* stack. If *erRecOn* is false, *erRollBack* simply returns the usual error code.

These macros are for illustration only. Thus, there are no internal checks for problems, and you should define the global data structures as static values in a library module or create a structure to collect them. This structure is passed to each of the transaction error-handling functions.

**Listing 4** contains wrapper macros that cause the program to call the functions in the file *e.c* in place of the standard library functions. The functions in *e.c* behave the same as the standard library functions, but if the error transaction manager is on (*erRecOn* is true in *erpub.h*), control passes to the last defined rollback point, rather than just returning the same error code as the associated standard library function.

Using these wrapper macros makes it easier to add transaction error handling to old programs, but if you want to

**LISTING 4 - WRAPPER MACROS**

```
/*epub.h - Error Library Wrapper Macros (only a few are
           shown here) */
#define ceEOF           1
#define ceOutOfMem      2
#define ceReadErr       3
#define ceReadShort     4

#ifndef vInE
#define fclose(pStream)                         eClose(pStream)
#define fopen(pFileName, pType)                 eOpen(pFileName, pType)
#define fread(pPtr, pSize, pNItem, pStream) \
        eRead(pPtr, pSize, pNItem, pStream)
#define fseek(pStream, pOffset, pPrtName) \
        eSeek(pStream, pOffset, pPrtName)
#define malloc(pSize)                           eMalloc(pSize)
#endif
```

**LISTING 5 - WRAPPER FUNCTIONS**

```
/* e.c - Error Library Wrapper Functions (only a few are
         shown here) */
#define   vInE
#include      "epub.h"
void *  eMalloc(pSize)
        size_t pSize;
{
        void *  Mem;
        if ((Mem = malloc(pSize)) == NULL) {
                erRollBack("malloc", ceOutOfMem, Mem);
        }
        return(Mem);
} /*    eMalloc */
size_t  eRead(pPtr, pSize, pNItem, pStream)
        char * pPtr;
        size_t pSize, pNItem;
        FILE * pStream;
{
        size_t Num;
        Num = fread(pPtr, pSize, pNItem, pStream);
        if (feof(pStream)) {
                erRollBack("fread", ceEOF, Num);
        } else if (Num <= 0) {
                erRollBack("fread", ceReadErr, Num);
        } else if (Num < pNItem) {
                erRollBack("fread", ceReadShort, Num);
        }
        return(Num);
} /* eRead   */
```

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make the error-handling process more visible, have the program call the functions in *e.c* directly instead of the standard library functions. The file in **Listing 4** is also a good place to define context-independent error codes.

The file in **Listing 5** contains the implementations of the wrapper macros in *epub.h*. **Listing 5** shows only two of the functions. These functions behave exactly like the standard library functions with the same name because they call the standard library functions. For more flexibility, a real error transaction manager might allow you to define the error codes that determine whether a rollback occurs.

So far, only small programs and enhancements of existing programs have used the transaction error-handling technique. But, its features—greater code reuse, greater code supportability, and better quality code—may make it more widespread. Just as you can separate the functional part of algorithms from user interfaces (client/server models), you can also separate error handling from the functional algorithm. EDN

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*Bruce A Rafnel is a software engineer at the Professional Services Division of Hewlett-Packard Co, Mountain View, CA, where he has worked for 12 years. In his current position, he develops Standard General Markup Language (SGML) applications that help deliver HP's customer-training courses. Rafnel also helped develop the Charting Gallery graphics package for PCs and internal SGML applications, and he helped enhance the VPlus forms manager for HP3000 Unix systems. He earned a BS in computer science at California Polytechnic State University at San Luis Obispo. A member of the IEEE and the C Users Group, Rafnel lists voice-controlled home automation as one of his spare-time interests.*

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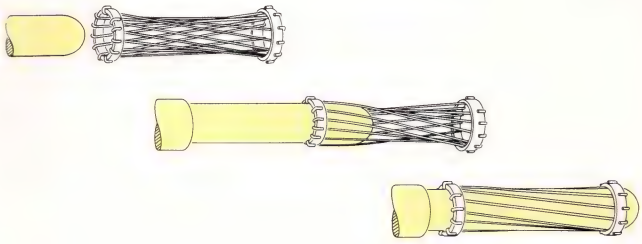

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# Designing with hysteretic current-mode control

Gedaly Levin and Kieran O'Malley, Cherry Semiconductor Corp

***Hysteretic current-mode control has many advantages over constant-frequency control, including stability, inherent load-current limiting in a buck topology, and an instantaneous response to load-current changes.***

Since the first current-mode control ICs emerged in the early 1980s, the popularity of current-mode control has made it the method of choice for most power supplies. Although there are a number of different types of current-mode control (**Ref 1**), the most popular is constant frequency with turn on at clock time. Constant-frequency control has become synonymous with current-mode control for most designers. As a result, the most popular control ICs are the 384X series, which a variety of suppliers manufacture.

Although the limitations of constant-frequency control are well known, it has remained the dominant control method for just about 10 years. Other methods, such as resonant-mode control, have not become as popular as expected, perhaps because of the difficulty in designing a practical supply and an overwhelming fear of variable switching frequencies within the power community. Industry focus recently has shifted to power-factor correction because of the impending implementation of IEC 555 and to synchronous switching for maximum efficiency. Still other methods of current-mode control remain unexplored.

One of the alternate types of current-mode control for which control ICs are available is hysteretic-mode control. Hysteretic current-mode control, which the Bose Corp patented in 1984 (**Ref 2**), has remained an obscure technique few designers use, yet it offers significant advantages for many applications. Hysteretic current-mode control (HCMC) offers the tightest and most accurate control of inductor current, is unconditionally stable regardless of duty cycle, and offers excellent transient response to step loads. The advantages of this control technique include

- Inherent load-current limiting
- Short-circuit-proof operation in buck-derived topologies
- No slope compensation required for duty cycles above 50%
- Easy loop-stability design
- No subharmonic oscillation
- Instantaneous response to load-current changes
- Constant peak-to-average inductor-current ratio.

Also, because the off time extends as the output voltage drops, the average power dissipated across the switch is always under control.

You can use HCMC with most switching-regulator topologies, including buck, forward-mode, boost, and continuous-mode flyback converters (see **box,** "Buck-regulator design example," which takes you through a typical design step by step).

HCMC ideally suits applications that require control of both load current and output voltage and require that power supplies behave as constant-current sources and as constant-voltage regulators. Examples of these applications include

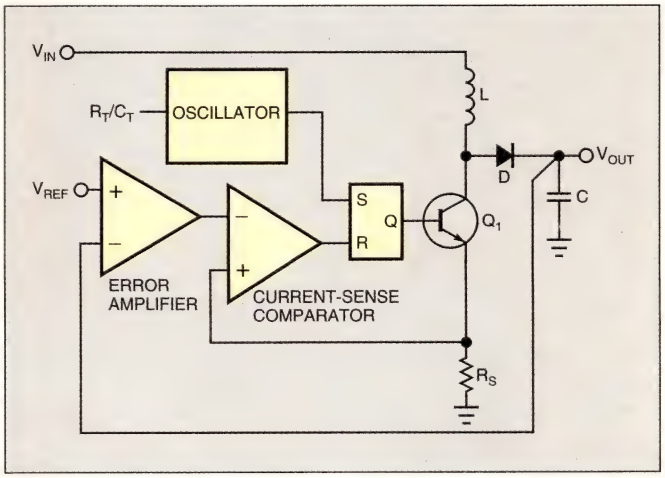


**Fig 1—An external R/C network determines the fixed operating frequency of a constant-frequency controller; the control loop determines the on-time of $Q_1$.**

## HYSTERETIC CURRENT-MODE CONTROLS

battery chargers, arc welders, fluorescent lamps, laser power supplies, and servo-motor control circuits.

Due to its free-running operation, HCMC is unsuitable for any application that needs to synchronize the supply's switching frequency with some external clock. This frequency variation, while predictable, may also limit HCMC's application in certain areas, such as video. Although not discussed in this article, HCMC can provide pulse-by-pulse overcurrent protection in universal-input power supplies that use a continuous-mode flyback topology.

### Compare constant frequency vs hysteretic

Comparing the operation of constant-frequency and hysteretic-mode controllers highlights major differences. **Fig 1** shows a simplified block diagram of a constant-frequency current-mode regulator. The clock or oscillator sets the RS flip-flop each cycle and turns on power-switch $Q_1$ while the control loop determines the period for which it remains on. The external $R_T/C_T$ network determines the operating frequency.

In **Fig 1**, the controller detects the peak inductor current by sampling the voltage across $R_S$ while sampling the output voltage $V_{OUT}$ directly. Depending on the value of $V_{OUT}$, the output of the error amplifier determines the peak current that flows in the inductor by constantly adjusting the voltage level on the inverting terminal of the current-sense comparator. The controller detects any change in the input voltage by detecting a change in the peak current measured as a voltage across $R_S$; it then adjusts the on-time of the FET to hold $V_{OUT}$ constant.

This common configuration has several disadvantages. First, regulation performance is limited because the switch turn-on is always controlled by the clock and is independent of the feedback loop. Thus, a minimum on-time exists, which limits the maximum operating frequency and can become a significant part of the total switching period.

A second problem with this configuration also occurs: Because the circuit only detects the peak current, the peak-to-average current error will vary with duty cycle. **Fig 2** shows what happens in a fixed-frequency controller when an increase in input voltage causes a change in the duty cycle (assuming a constant output voltage). Time, $t_1$ stands for the on and off times that correspond to some low input voltage, and $t_2$ to some higher input voltage. The down slope of the inductor current is constant and equal to $V_{OUT}/L$.

When $V_{IN}$ is low, more time is required for the current to reach its peak value $I_{PEAK}$, which results in a higher average current ($I_{AVG1}$ in **Fig 2**). On the other hand, if the input voltage is high, the on-time is reduced, and the average current, $I_{AVG2}$, is lower. Thus, the peak-to-average current ratio depends on the duty cycle. Because the output voltage is proportional to the average current, changes in the input voltage cause momentary changes in the output voltage—which the error amplifier feedback loop corrects. The current-sense-amplifier loop monitors the peak current and causes a further output-voltage change.

A third problem with a fixed-frequency system is that it can become unstable for duty cycles greater than 50%. Any increase in inductor current ($\Delta I_1$ in **Fig 3**) tends to increase with time if the duty cycle is greater than 50%, resulting in a larger increase, $\Delta I_2$. Slope compensation can overcome this problem but adds complexity and external components to the design.

### Hysteretic current-mode control

**Fig 4a** shows a similar regulator that uses a hysteretic-mode control system. In HCMC, no oscillator exists. The regulator senses inductor current by monitoring the voltage across $R_S$ using a differential current-sense amplifier. This amplifier's output drives two comparators, $I_{PEAK}$ and $I_{VALLEY}$. The inductor current $I_L$ ramps alternately between an upper limit $I_{PEAK}$ and a lower limit $I_{VALLEY}$ (**Fig 4b**).

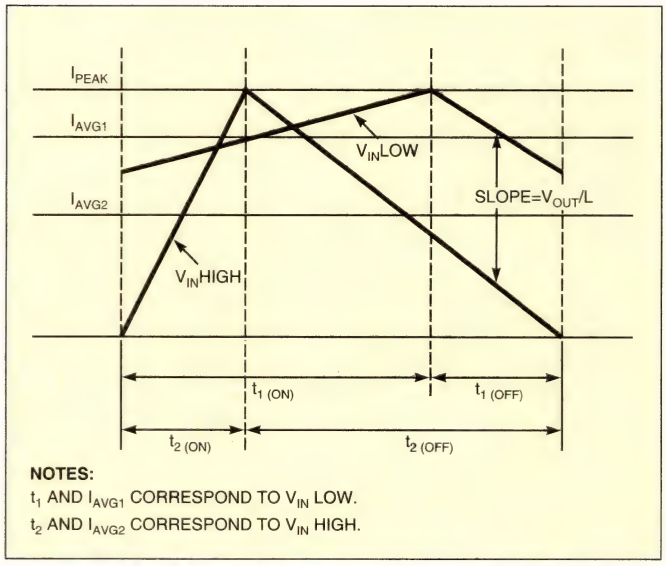


**Fig 2—One disadvantage of fixed-frequency control is that changes in input voltage cause changes in the duty cycle. Duty cycle changes, in turn, cause changes in the peak-to-average current ratio.**

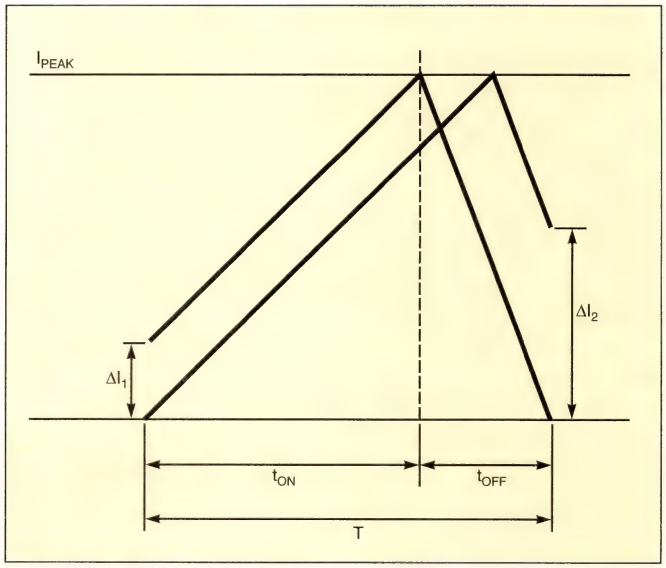


**Fig 3—In fixed-frequency controllers with duty cycles greater than 50%, the response to an input-current change $\Delta I_1$ is a larger change $\Delta I_2$.**

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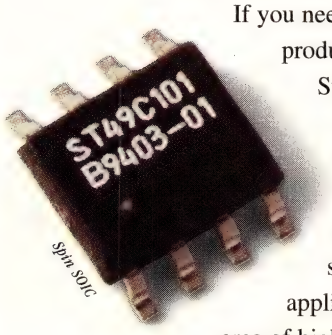


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## HYSTERETIC CURRENT-MODE CONTROLS

The hysteretic-mode regulator (typically implemented in a control IC such as the CS324) maintains a controlled difference ΔI between the comparators' inputs using a voltage-controlled current source (VCCS). The output of an error amplifier adjusts the reference voltage on the inverting terminal of the $I_{PEAK}$ comparator depending on the value of $V_{OUT}$. The peak and valley comparators' output controls the RS flip-flop, which turns the transistor switch off and on. If $V_{OUT}$ changes, the reference voltage for $I_{PEAK}$ changes and the reference point for $I_{VALLEY}$ follows, thereby keeping the current-hysteresis band ΔI constant.

As the inductor current increases, the output of the current-sense amplifier reaches the threshold of comparator $I_{PEAK}$ whose output goes high, which resets the flip-flop and turns off $Q_1$. As the inductor current ramps down, the output of the current-sense amplifier decreases to the threshold of comparator $I_{VALLEY}$. The output of this comparator then goes high, the flip-flop sets, and $Q_1$ turns back on.

**Fig 5** shows what happens when the input voltage to an HCMC supply increases. As in **Fig 2**, $t_1$ and $t_2$ correspond to low and high input voltages. When the input voltage is high, the switch-on time ($t_{2(ON)}$) decreases, which is similar to fixed-frequency control. However, the hysteresis band ΔI remains constant, as does the discharge slope, which ultimately increases the switching frequency, because $f_2=1/t_2$. Thus, unlike constant-frequency control, the peak-to-average current difference does not vary with duty cycle.

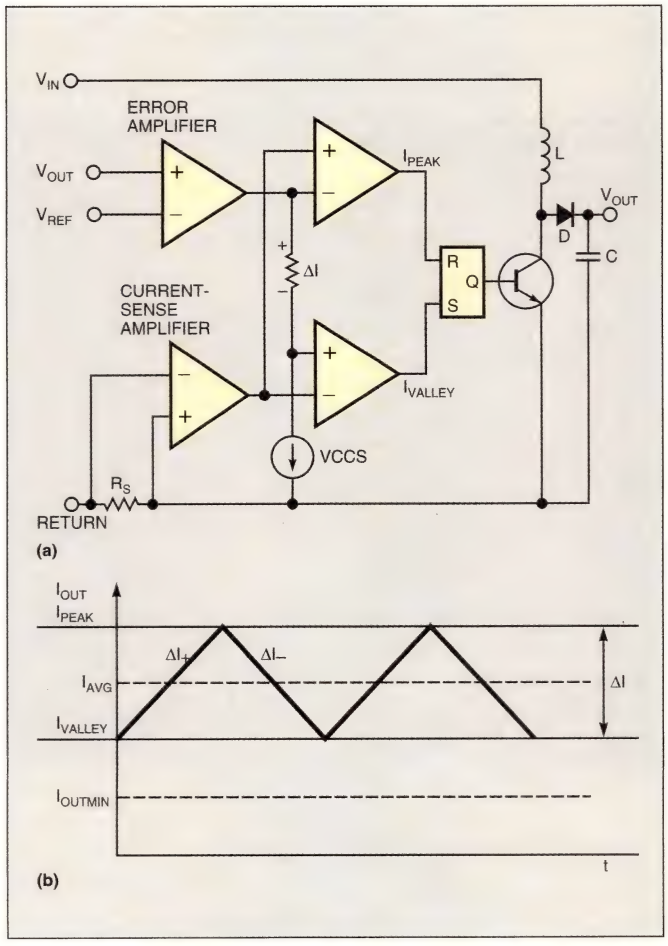



**Fig 4—A hysteretic-mode controller (a) maintains a difference (ΔI) between two comparators, and inductor current increases and decreases between the comparators' $I_{PEAK}$ and $I_{VALLEY}$ thresholds (b).**

### Hysteretic control provides stability

HCMC also overcomes the instability problem associated with fixed-frequency operation for duty cycles above 50% without the need for slope compensation. An increase in load current $\Delta I_1$ causes the fixed hysteresis band ΔI to move upward by an amount $\Delta I_1$ (**Fig 6**), which means that the disturbance at the end of the cycle ($\Delta I_2$) is the same as at the beginning. Thus, HCMC remains stable regardless of duty cycle.

Another benefit of HCMC is its ability to limit the short-circuit current in buck or buck-boost converters. When the output of a buck regulator (**Fig 7**) short circuits and $Q_1$ is on, $V_{OUT}=0V$, and the voltage across the inductor equals $V_{IN}$. The inductor current rises quickly and reduces $t_{ON}$ (**Fig 8**). The discharge time $t_{OFF}$ also increases because it is determined by $V_{OUT}/L$, and $V_{OUT}$ is effectively a short circuit. The only voltage across the inductor during $t_{OFF}$ is the forward voltage drop $V_D$ of the diode. $Q_1$ doesn't turn on again until the current has dropped to the required valley limit. Thus, under short-circuit conditions, an HCMC regulator can only deliver a fixed maximum current.

### Derive design equations

In **Fig 7**'s basic buck regulator, $Q_1$ interrupts the input voltage and provides a variable-duty-cycle and variable-frequency square wave to the output LC filter. The filter averages the square waves to produce a dc output voltage. The ΔI hysteresis-band setting controls the inductor current; the voltage-feedback loop controls the output voltage. The average voltage across the inductor over one cycle is zero. The volt-time product of $t_{ON}$ must equal that of $t_{OFF}$.

A number of equations are crucial to the design of a hys-

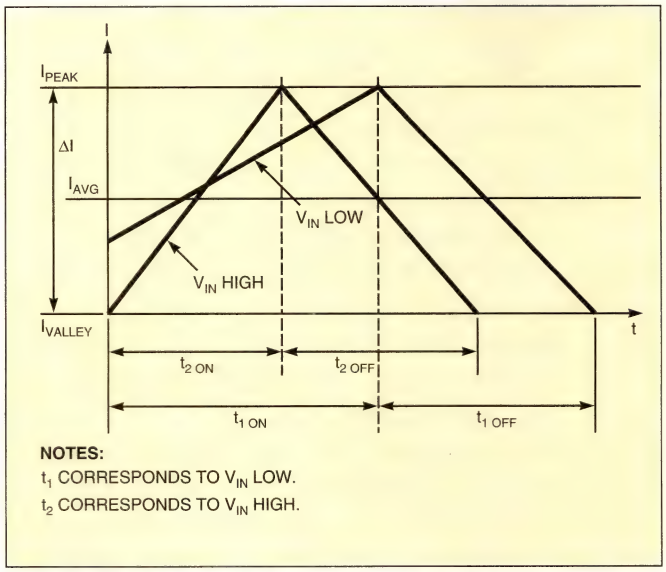
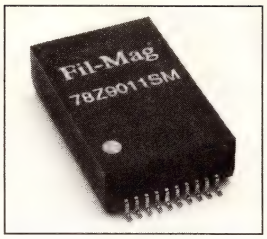



**Fig 5—With HCMC, the peak-to-average current remains constant regardless of input voltage.**

## 100Base-VG Module for Emerging IEEE 802.12 Standards

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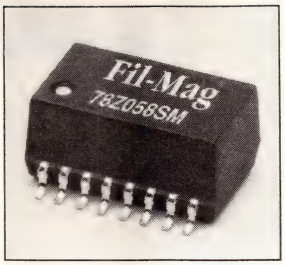
## Magnetics for 100Base-T and TP-PMD

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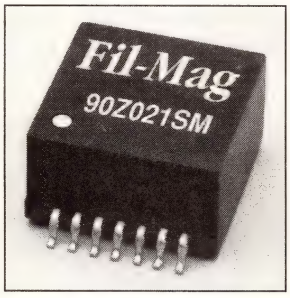


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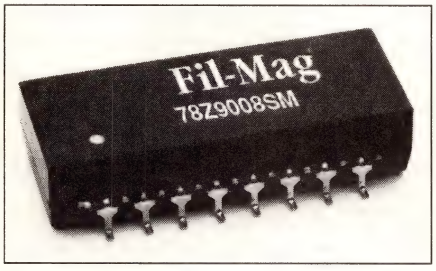


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## HYSTERETIC CURRENT-MODE CONTROLS

teretic-mode regulator. During the on and off times, the voltage across the inductor L is given by the following equations, respectively, where $V_{DS}$ is the FET's drain-to-source voltage and $V_D$ is the diode's forward voltage drop:

$$V_{L+} = V_{IN} - V_{OUT} - V_{DS} \quad (1)$$

$$V_{L-} = V_{OUT} + V_D. \quad (2)$$

$$\text{Also, } V_{L+} \times t_{ON} = V_{L-} \times t_{OFF} \quad (3)$$

$$\text{and } V_{OUT} = V_{L+}\left(\frac{t_{ON}}{t_{OFF}}\right) - V_D. \quad (4)$$

In a hysteretic buck regulator, the fixed hysteresis band ΔI controls the ac current through the inductor. If $\Delta I_+$ is the up slope and $\Delta I_-$ is the down slope of the inductor current in **Fig 4b**, then

$$\Delta I_+ = \Delta I_- = \Delta I. \quad (5)$$

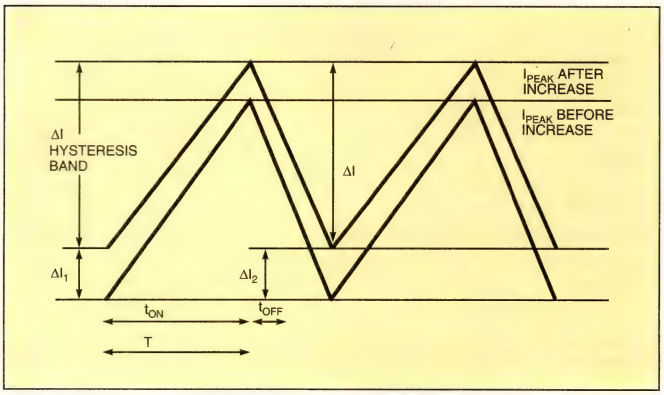



**Fig 6—Hysteretic controllers are inherently stable because increases in load current simply shift the hysteresis band upward, leaving the current disturbance unchanged at the end of one cycle.**

During the on-time,

$$\Delta I_+ = \frac{(V_{IN} - V_{OUT} - V_{DS})t_{ON}}{L} \quad (6)$$

## BUCK-REGULATOR DESIGN EXAMPLE

The design starts with a known set of requirements. For this example, $V_{IN}$=9 to 14V dc, $V_{OUT}$=5V dc, ±1%, $I_{OUTMAX}$=2A, $I_{OUTMIN}$=0.2A (10% of full load), and switching frequency= 200 kHz at maximum input voltage.

(**1**) Choose a value for the hysteresis current ΔI based on the minimum load conditions using **Eq 12** (from text):

$$\Delta I = 2 \times I_{OUTMIN} = 2 \times 0.2A = 0.4A.$$

(**2**) Calculate the value of $R_{SENSE}$ using **Eq 14**:

$$R_{SENSE} = \frac{V_{SENSEMAX}}{I_{OUTPEAK}} = \frac{0.5}{2.2} = 0.227\Omega = 0.2\Omega \pm 10\%.$$

(**3**) Choose the inductor value for continuous operation at minimum load using **Eq 11**.

$$L = \frac{V_{OUT}}{f \times \Delta I}\left(1 - \frac{V_{OUT}}{V_{IN}}\right).$$

Thus,

$$L_{CRITICAL} = \frac{V_{OUT}}{f \times \Delta I}\left(1 - \frac{V_{OUT}}{V_{INMAX}}\right) = 40.2\,\mu H.$$

Allowing a 5% tolerance on the inductor value, $L_{CRITICAL}$=43 μH ±5%.

(**4**) Calculate the hysteresis voltage $V_{\Delta I}$ using **Eq 14** and **Eq 15**

$$V_{\Delta I} = 5 \times R_{SENSE} \times \Delta I = 0.4V.$$

(**5**) Determine minimum and maximum frequency of operation using **Eq 11**

$$f_{MIN} = \frac{V_{OUT}}{L \times \Delta I}\left(1 - \frac{V_{OUT}}{V_{INMIN}}\right) = \frac{5}{43\,\mu H \times 0.4A}\left(1 - \frac{5V}{9V}\right) = 129\ kHz$$

$$f_{MAX} = \frac{V_{OUT}}{L \times \Delta I}\left(1 - \frac{V_{OUT}}{V_{INMAX}}\right) = \frac{5}{43\,\mu H \times 0.4A}\left(1 - \frac{5V}{14V}\right) = 187\ kHz.$$

(**6**) Design the gate-drive circuit.

An N-channel FET is a better choice for the high-side switch because it has a lower $R_{DS(ON)}$, is less expensive, and has a wider selection available than for a comparable p-channel FET. However, the catch with using an n-channel device as a high-side switch is that it requires a gate-drive voltage. The circuit can easily generate this voltage if you add an additional winding to the main inductor. Because one end of the secondary winding is connected to the input voltage and the other to $V_{CC}$, the secondary voltage will remain above $V_{IN}$, providing a reliable gate-drive voltage. The steady-state voltage across the secondary winding is

$$V_{SEC} = V_{GS} = \frac{N_{SEC}}{N_{PR}}(V_{OUT} + V_{D(PR)}) - V_{D(SEC)},$$

where $V_{D(PR)}$ is the voltage drop across the primary diode and $V_{D(SEC)}$ is the voltage drop across the secondary diode. The turns ratio in this design is 1:1, and $V_{D(PR)}$ and $V_{D(SEC)}$ are equal, so $V_{GS}$=5V.

(**7**) Calculate the maximum power dissipation in the diode and FET.

If you short the output during the on-time, the regulator applies almost all of the input voltage to the inductor. However, a short during the off-time only applies the

and, during the off-time,

$$\Delta I_{-} = \frac{(V_{OUT} + V_D)t_{OFF}}{L}. \quad (7)$$

Solving for $t_{ON}$ and $t_{OFF}$ produces the following equations:

$$t_{ON} = \frac{\Delta I \times L}{(V_{IN} - V_{OUT} - V_{DS})} \quad (8)$$

$$t_{OFF} = \frac{\Delta I \times L}{(V_{OUT} + V_D)}. \quad (9)$$

Because the total cycle time $T=t_{ON}+t_{OFF}$ and switching frequency $f=1/T$,

$$f = \frac{1}{\Delta I \times L} \times \frac{(V_{IN} - V_{OUT} + V_{DS})(V_{OUT} + V_D)}{(V_{IN} - V_{DS} + V_D)}. \quad (10)$$

Finally, because $V_D$ and $V_{DS}$ are small compared with the other parameters in this equation, you can drop them and simplify the expression, ultimately leaving

$$f = \frac{V_{OUT}}{\Delta I \times L}\left(1 - \frac{V_{OUT}}{V_{IN}}\right). \quad (11)$$

Thus, under steady state conditions, the switching frequency is a function of $V_{IN}$ alone because $\Delta I$, L, and $V_{OUT}$ are constant.

**Solve for hysteresis-band current**

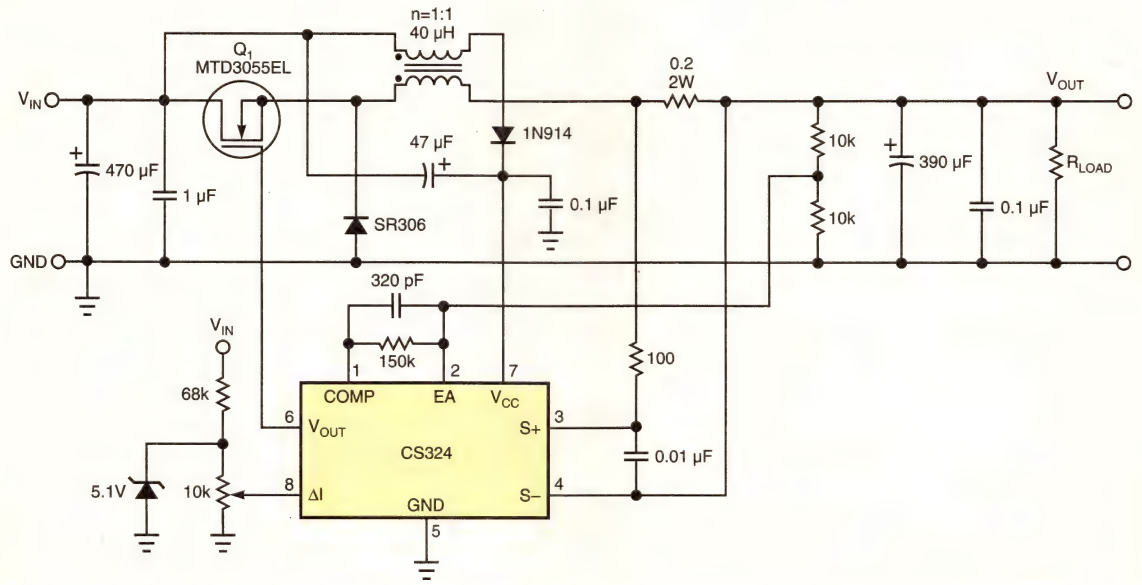
The average-inductor current $I_{AVG}$ has a fixed relationship to the peak-inductor current $I_{PEAK}$ regardless of duty cycle, and $I_{AVG}$ is related linearly to the hysteresis voltage $V_{\Delta}I$. The hysteresis voltage determines the width of the current hysteresis band in **Fig 4b**, which, along with the inductor, determines the boundary condition between continuous and discontinuous modes of operation and thus the minimum load conditions.

A good approximation for $\Delta I$, to allow for some forward-diode-drop voltage to the inductor. The design must fulfill the familiar $+\Delta I=-\Delta I$ balance requirement. Thus,

$$t_{ON(SC)} = \frac{L \times \Delta I}{V_{INMAX} - V_D} = \frac{43\ \mu H \times 0.4}{14 - 0.5} = 1.27\ \mu SEC$$

$$t_{OFF(SC)} = \frac{L \times \Delta I}{V_D} = \frac{43\ \mu H \times 0.4}{0.5} = 34.4\ \mu SEC.$$

You can use these values of short-circuit on and off times to calculate the worst-case power dissipation and power rating for the diode and FET during short-circuit conditions.




**This buck regulator's schematic details a complete design that uses hysteretic current-mode control.**

## HYSTERETIC CURRENT-MODE CONTROLS

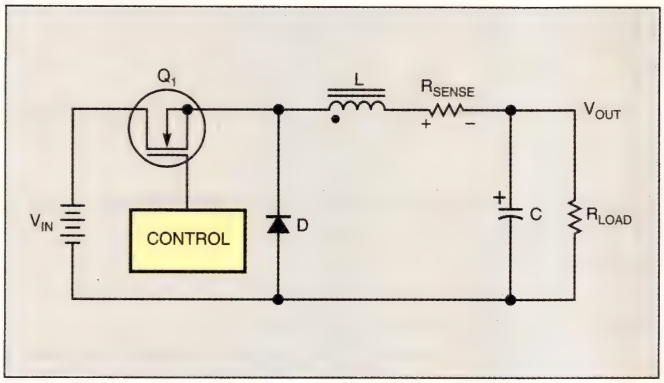



**Fig 7—In this basic buck regulator, the hysteresis band controls the inductor current, and a voltage-feedback loop controls the output voltage.**

headroom before discontinuous operation begins, is

$$\Delta I = 2 \times I_{OUTMIN}. \quad (12)$$

The relationship between the maximum output current $I_{OUTMAX}$ and the peak inductor current $I_{PEAK}$ (note that $I_{OUTMAX}$ is the same quantity as $I_{AVG}$ in **Fig 4b**) is

$$I_{OUTMAX} = I_{PEAK} - \frac{\Delta I}{2}. \quad (13)$$

Sense resistor $R_S$, which connects across the inputs to the current-sense amplifier, determines the maximum current the regulator can deliver. The relationship between $R_S$ and the maximum voltage developed across this resistor, $V_{SENSEMAX}$, is

$$I_{PEAK} = \frac{V_{SENSEMAX}}{R_{SENSE}} = \frac{0.5}{R_{SENSE}}. \quad (14)$$

$V_{SENSEMAX}$ has both a steady-state component due to $I_{OUTMAX}$ and a varying component due to $\Delta I$, which is determinedby the hysteresis voltage $V_{\Delta I}$. This varying component of $V_{SENSEMAX}$ is related to $V_{\Delta I}$ depending on the particular IC control you use. In the case of the CS324 control IC, $V_{SENSE}$ is related to $\Delta I$ (pin 8) by the relationship:

$$V_{SENSE} = \frac{V_{\Delta I}}{5}. \quad (15)$$

EDN

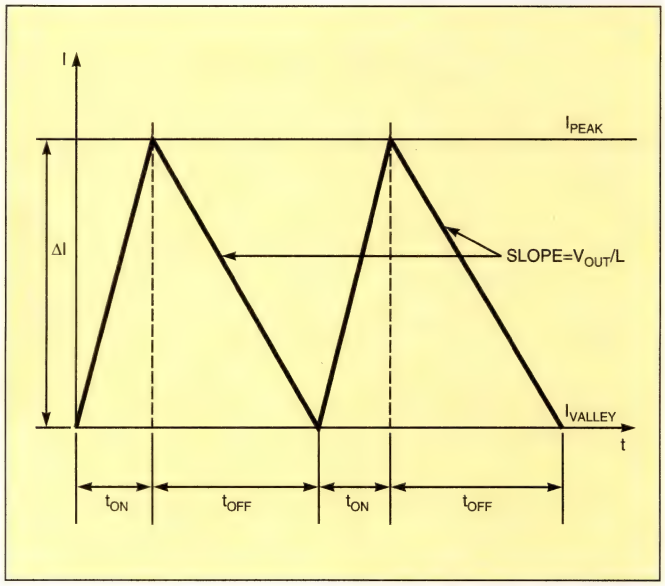



**Fig 8—Under short-circuit conditions, a fixed maximum current exists, $I_{PEAK}$, which hysteretic controllers can deliver.**

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*Gedaly Levin is a senior applications engineer for Cherry Semiconductor and has worked at the company for two years. He earned an MSEE from the Polytechnical Institute of Tallinn, Estonia.*

*Kieran O'Malley has five years of experience with Cherry Semiconductor, most recently as an applications engineer. He holds a BSEE from the University of Limerick in Ireland.*

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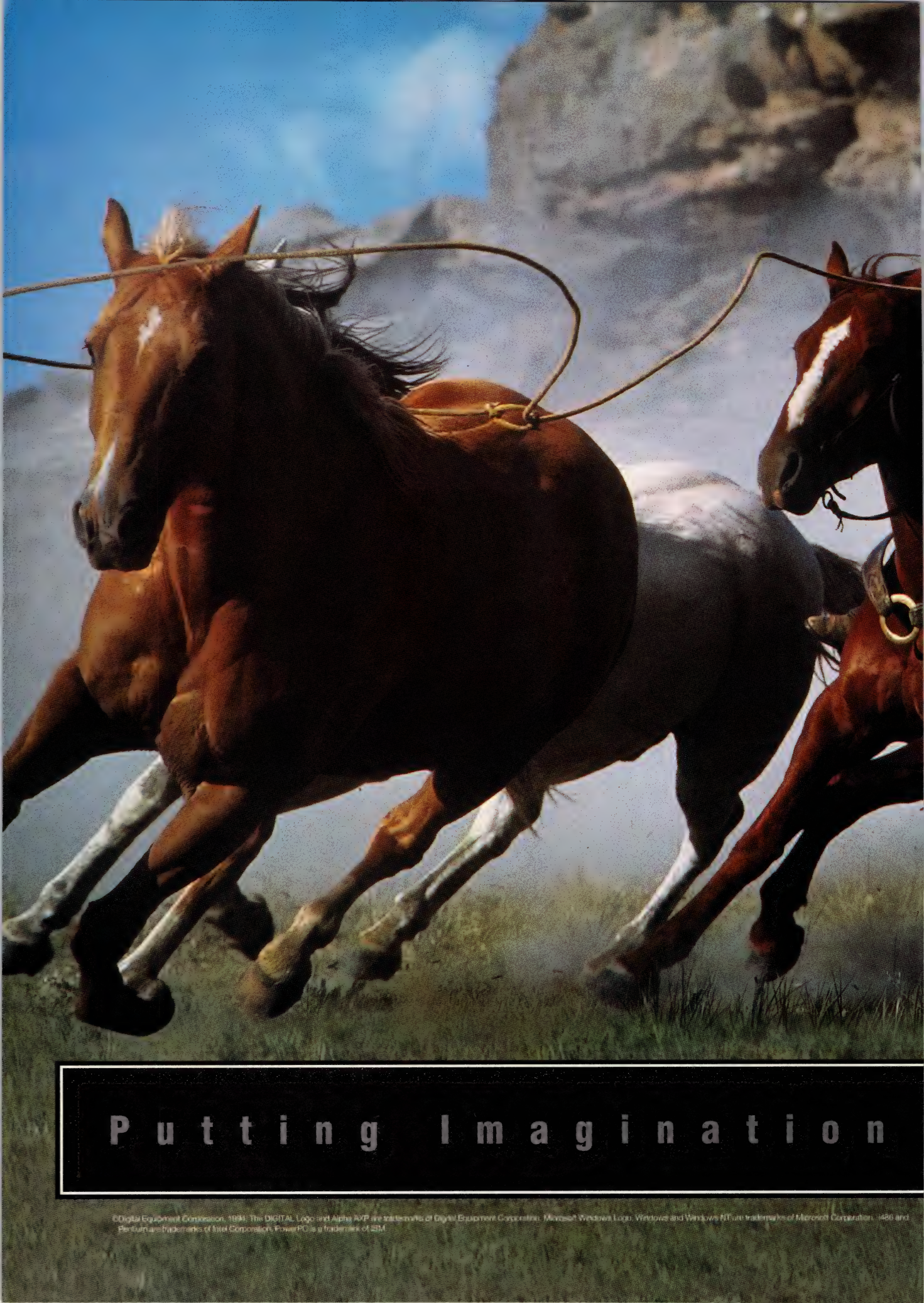

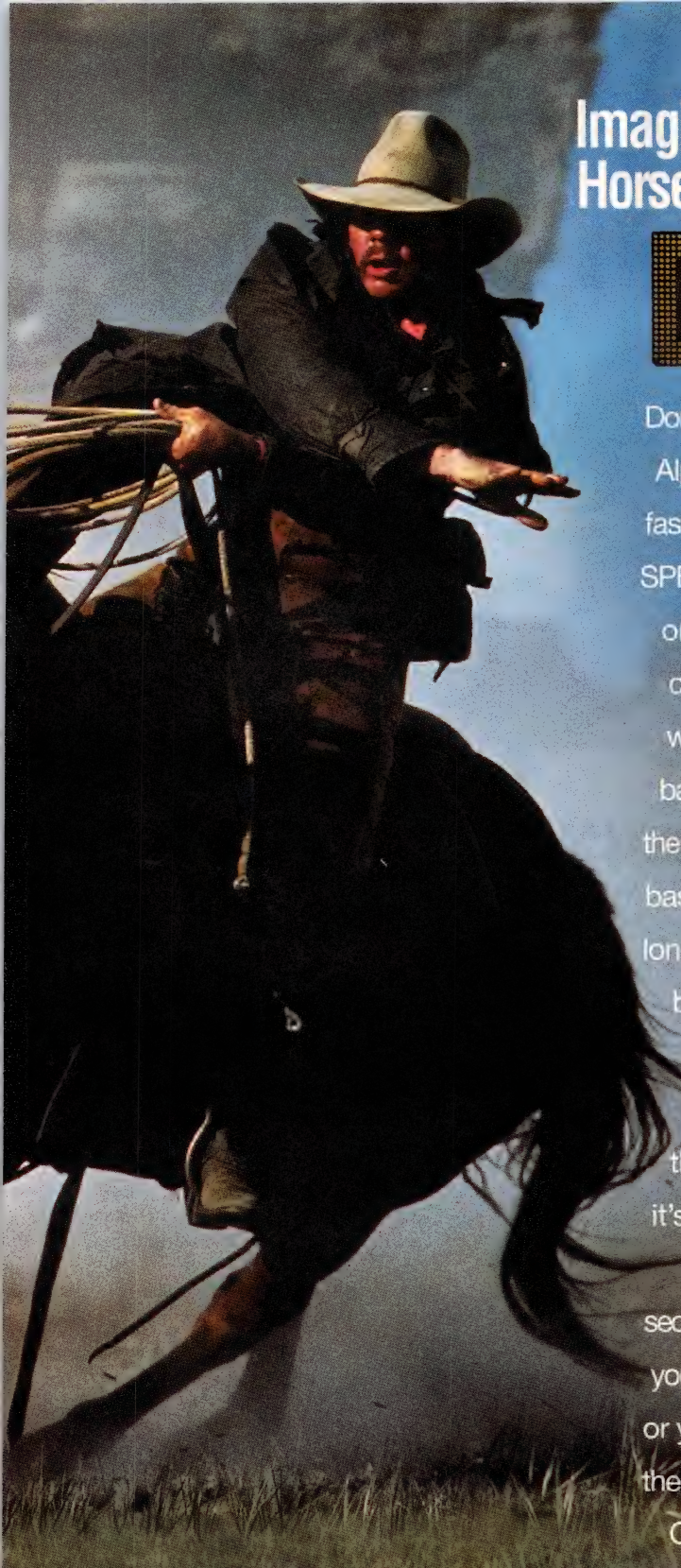

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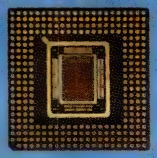
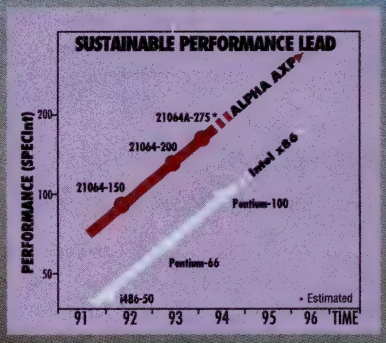


Windows NT™ puts tremendous power behind demanding corporate applications. Don't compromise it. Go with the front-runner — the Alpha AXP™ microprocessor. Choose from a family of fast microprocessors with performance as high as 170 SPECInt (est.) that leaves the fastest Pentium™ or PowerPC™ in the dust, yet is priced to compete. Alpha AXP runs Windows NT with unbridled speed, with hundreds of Windows NT-based applications shipping now and hundreds more on the way. Plus Alpha AXP runs MS-DOS and Windows™-based applications. And that's just the beginning of a long-term architecture based on a scalable RISC design and standards like the PCI local bus. And it's available to any PC maker—from us now, and later this year from our second source Mitsubishi Electric Corp. With Windows NT, you have a choice. You can hang back with the herd, or you can choose Alpha AXP. And cut loose. So put the spurs to your PC maker. Ask them about Alpha AXP. Or call us at 1-800-332-2717. Your future is riding on it.

MICROSOFT WINDOWS NT COMPATIBLE

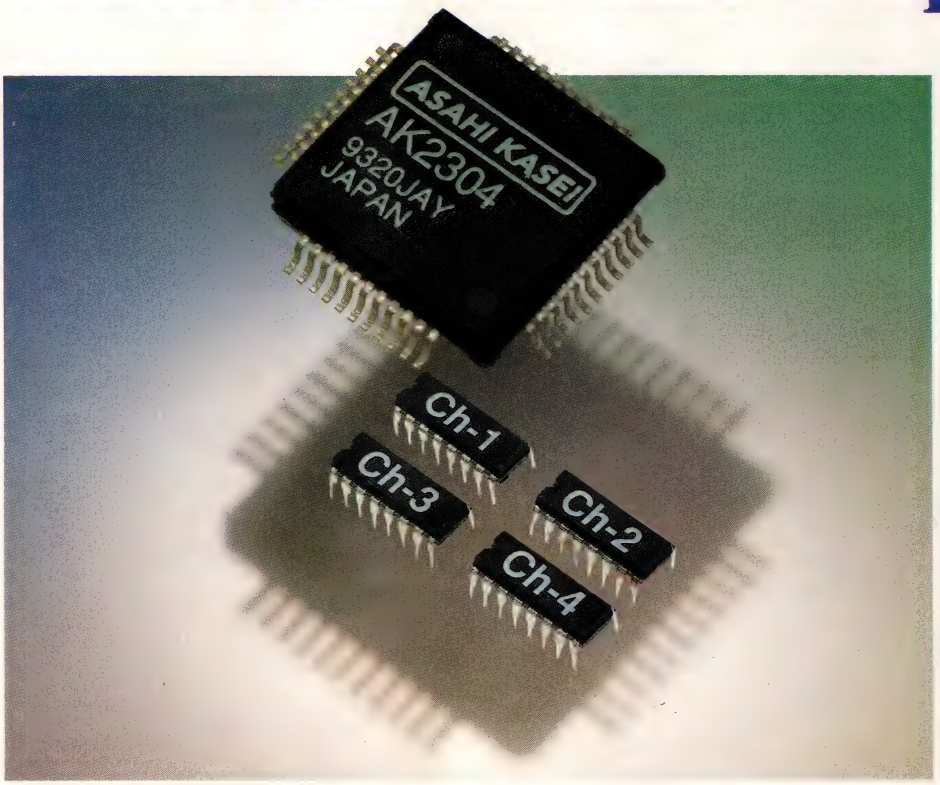



To Work digital™

CIRCLE NO. 98

AKM

# AK2304
# 4 channels on one chip.

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- OP-amp for input gain adjustment and anti-alia filtering
- 2,048 MHz PCM data transmission rate
- Separate mute each channel
- Power down mode
- Single +5V ±5% operation
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AKM

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CIRCLE NO. 99

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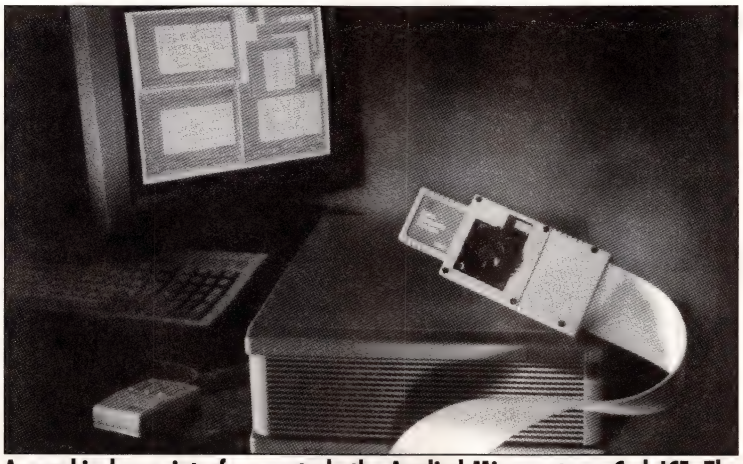
# 40-MHz ICE for the 68040 operates as fast as 40 MHz

In a move to lower the cost of high-end in-circuit emulation, Applied Microsystems bases its CodeICE in-circuit emulator (ICE) family on a single-board architecture. The first member of a family, CodeICE 040, works with the Motorola 68040, 68EC040, and 68LC040 μPs at speeds up to 40 MHz.



**A graphical user interface controls the Applied Microsystems CodeICE. The device supports 40-MHz 68040 μPs.**

CodeICE includes a complex trace and event system, up to 4 Mbytes of optional overlay memory, a 136-bit-wide, 8k-word-deep (optional 32k-word-deep) trace memory, and a source-level debugger. The source-level debugger, a graphical user interface for the ICE, provides pull-down and pop-up menus to speed debugging. It also includes a "notebook" from which users can select subjects by clicking on "tabs," causing "pages" to appear showing all the options for a command.

CodeICE doesn't consume target resources. For example, it does not use nonmaskable or other interrupts. It runs at the full speed of the μP—now 40 MHz—and, like the μP, will operate faster in the future. When operating in target memory, the ICE does not insert wait states, even at clock speeds of 40 MHz, and the overlay memory does not need wait states at speeds as high as 25 MHz.

The device's fully isolated probe tips use FET-isolation technology for low skew, delay, and load. Ethernet (4 Mbytes/minute) or a high-speel parallel interface (5 Mbytes/minute) provide channels for uploads and downloads. CodeICE also offers diagnostic routines so that you can set up execution loops to snoop with a scope and see what the hardware is doing.

The CodeICE supports using a 68360 in companion mode with the 68040. A register utility supports the 68360's SIMM registers, and a decode utility decodes those registers. The device also supports cache coherency and bus snooping for multiple-68040 implementations.

CodeICE costs $20,950 for Sun 4 workstations. A Microsoft Windows version will be available in July for $19,950.**—David Shear**

*Applied Microsystems Corp, Redmond, WA. (206) 882-2000.*

**Circle No. 320**

# Debugger controls multiple processors simultaneously

The SuperVision debugger from Mercury Computer Systems lets you debug real-time systems based on multiple processors. Instead of using a single-processor debugger for each processor, SuperVision allows you to simultaneously monitor and control multiple processors. A graphical user interface (GUI) provides a system-level view of the embedded system. Through the GUI, you can debug one to hundreds of processors.

SuperVision's multiple monitoring capability lets you view the operation of each processor. Developed to support Mercury's Race multicomputers, SuperVisor accesses the runtime environment via the company's MC/OS distributed real-time operating system.

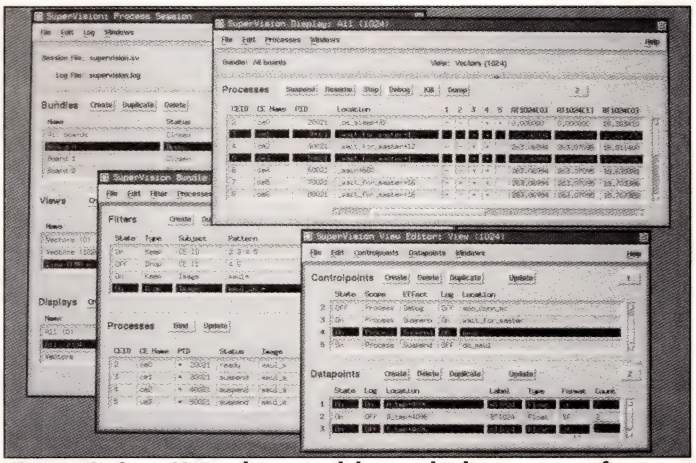
SuperVision offers a choice of four window types: a process session that lets you create other windows, a bundle editor that groups processes for monitoring and control, a view editor that handles bundle control and data processing, and a display window that presents a real-time interactive display of the multicomputer runtime environment.

Other tools available with SuperVision save and restore all debug and display setup parameters, log data during operation for off-line analysis, and provide on-line, context-sensitive help. SuperVision runs on Sun workstations; prices start at $5500.

**—David Shear**

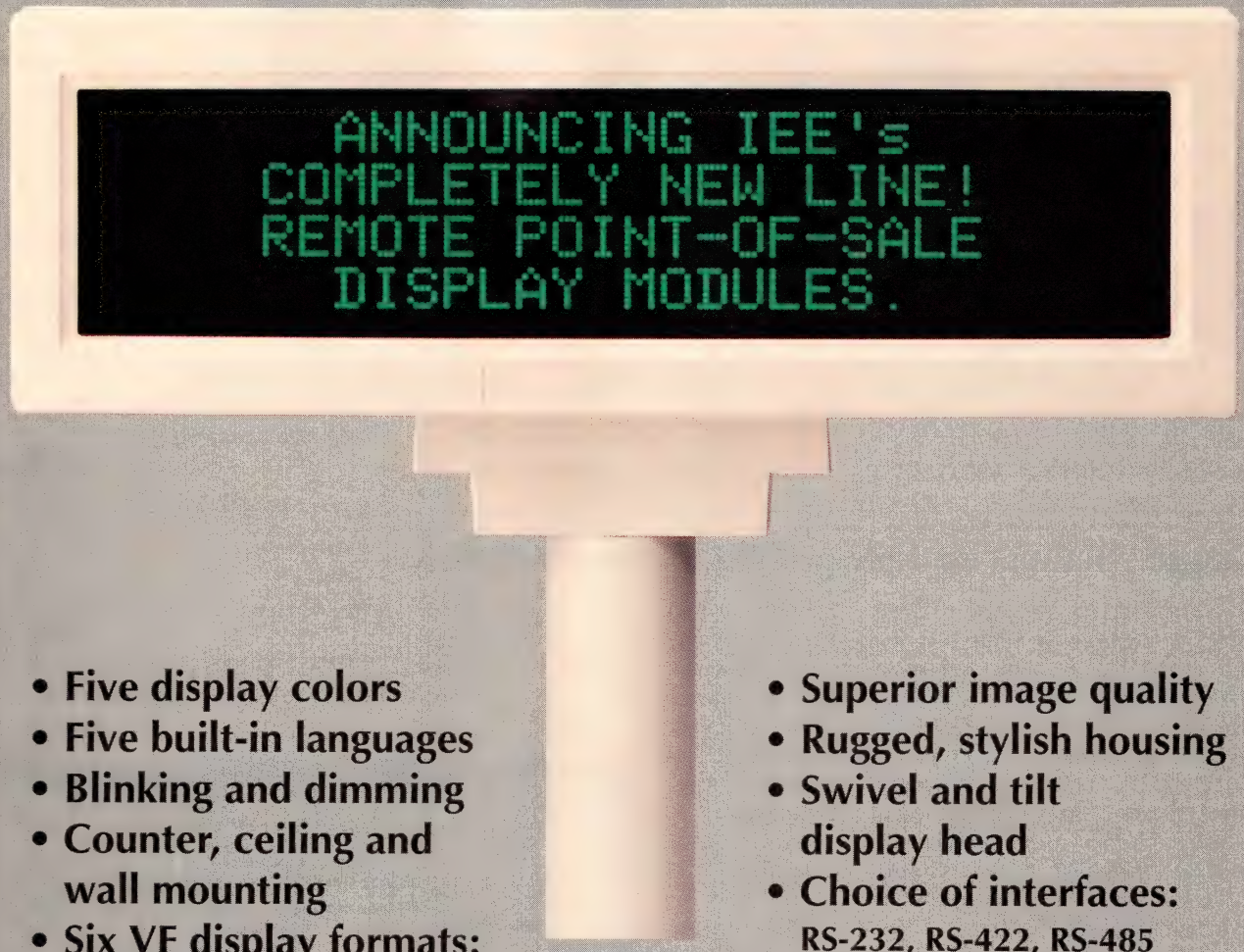
*Mercury Computer Systems Inc, Chelmsford, MA. (508) 256-1300.*

**Circle No. 321**



**Mercury's SuperVision lets you debug multiple processors from one debugger.**

# SEND A CLEAR MESSAGE!

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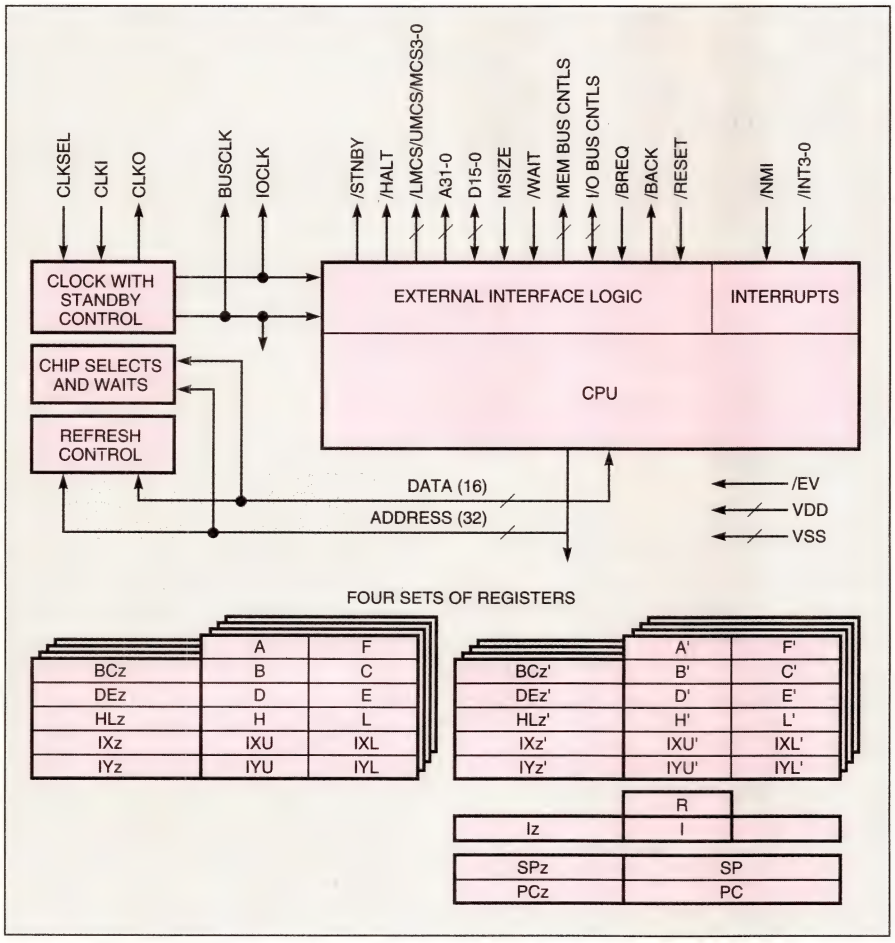
*Immediate Response Circle #100*
*Reference Only Circle #101*

# Zilog extends Z80 to 16 bits, 32-bit addressing




**The Z380 superimposes the Z80 instruction-set architecture on a 16/32-bit hardware implementation. The Z380 handles 16/32-bit operations and full 32-bit addressing. It has an on-chip DRAM controller to simplify design-in.**

**Zilog Z380 μP**

- 25-, 40-MHz clock (static design)
- 32-bit ALU
- 32-bit multiply, divide
- Two register sets with four banks each (8/16/32-bit registers)
- 8/16/32-bit operations
- 2-clock basic instruction cycle
- 16/32-bit SP, software stack
- 32-bit internal data bus
- 16- or 32-bit address space
- 16-bit external data bus
- DRAM controller: six chip selects, programmable wait states, refresh
- Sleep, standby modes
- Four external interrupts
- 2100-pin quad flatpack
- 2$10 (100,000)

The Zilog Z80 μP is alive and well. Based on a pioneering architecture descended from the Intel 8080, that Z80 has built a wide following in applications requiring a full 8-bit μP that can move data. Zilog has now introduced the Z380 μP, which extends the core Z80 architecture for 16-bit processing and 32-bit addressing. Using current design technology, the 16-bit μP supports clock rates up to 40 MHz.

The original Z80 was a silicon miser: To cut real estate, Z80 designers used a 4-bit adder and traded time for silicon. Many years later, the Z380 designers took advantage of today's higher silicon densities and advanced design techniques. Unlike the Z80's 4-bit data paths, the Z380 has full 32-bit data paths for 32-bit address and data calculations. It performs 8-, 16-, and 32-bit operations. The Z380 also extends the Z80's dual-register set to two register groups, each with four sets of registers. The device also extends the Z80 register set to 16- and 32-bit registers. You can use the Z380 register sets as register banks for fast context switching.

The Z380 takes two 40-MHz clocks to execute a basic instruction (100 nsec). Most instructions execute in three clock cycles. The Z380's hardware is semipipelined: It starts the next instruction fetch while finishing execution of the current instruction.

The Z380 is code-compatible with the Z80 and Z180 μPs; it can run Z80 and Z180 code with a 64-bit address space, and operate in extended mode with 32-bit addressing that opens memory to 4 Gbytes of address space. The chip offers a full set of addressing modes, including register, immediate, indirect register, direct, indexed, PC relative, and stack-pointer relative (new).

For easier design-in, the Z380 has an on-chip DRAM controller for off-chip memory. It supplies up to six chip-select signals and has a DRAM-refresh controller. Additionally, it takes up to four external maskable interrupts and one nonmaskable interrupt to interrupt processing for external events. Interrupt-response time is approximately 8 μsec.

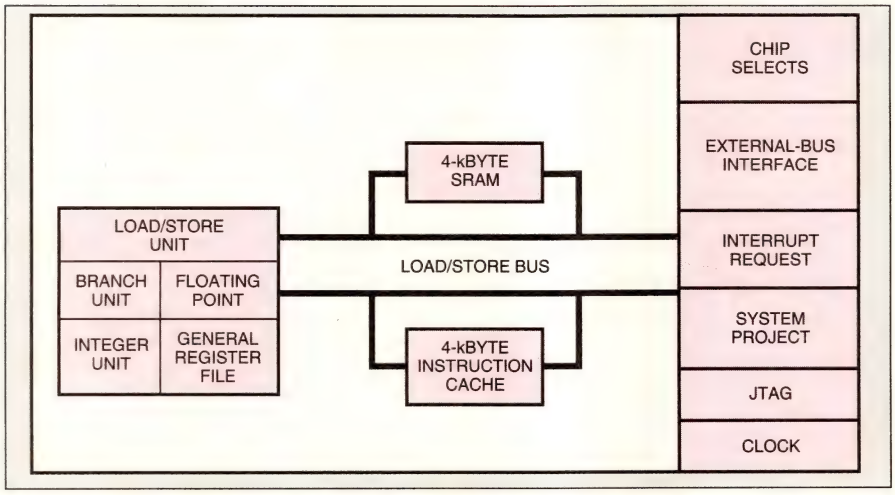
Zilog supplies an assembler, a linker/loader, and a C compiler with the Z380. Also available are an evaluation board and an in-circuit emulator.

**—Ray Weiss**

*Zilog Inc, Campbell, CA. (408) 370-8056.* **Circle No. 332**

# Motorola 32-bit PowerPC targets embedded control

Complex embedded applications, such as automotive-engine and drive-train control, are migrating to 32-bit processing. These applications are opening the door for 32-bit RISC processors to go beyond standard data-staging applications, such as laser printers, X-terminals, and communications servers. For example, Ford Motor Co has contracted with Motorola to develop an embedded version of the PowerPC architecture for engine and drive-train control.




**Motorola's embedded PowerPC controller, the RMCU505 delivers 25-MIPS peak performance at a 25-MHz clock rate. Motorola bases the μC on a single-issue architecture. The 505 has 4 kbytes of instruction cache and 4 kbytes of data SRAM.**

The resultant microcontroller (μC) family, Motorola's RMCU500, delivers a peak performance of 25 MIPS with a 25-MHz clock. Later versions will increase clock rates to 40 MHz, with a corresponding 40-MIPS peak performance.

The first family member, the RMCU505 is a single-instruction machine, unlike the mainstream PowerPC 600 series, which are superscalar processors and can issue more than one instruction/clock cycle. The 505 has a simplified 4-stage pipeline, a 4-kbyte instruction cache, and a 4-kbyte general RAM, unlike the PowerPC chips, which have a unified cache or separate instruction or data caches. For many embedded applications, the 505's inner-loop code can fit into the 1k-word instruction cache. The chip has a 32-bit external-memory interface to minimize memory costs. The external bus supports a 4-word burst mode to speed memory accesses.

The RMCU500 family is a Motorola-specific architecture that builds on the PowerPC Instruction Set Architecture, which Motorola developed with IBM and Apple Computer. The RMCU500 designers are taking advantage of Motorola's μC technologies. The RMCU500 family incorporates the next generation of the Intermodule bus developed for integrating multiple peripherals in the 32-bit 68300 μC family. This bus provides a standard, on-chip, intermodule connection for peripherals, making it easy for Motorola engineers to add peripherals or create application-specific variations.

Instruction-set-compatible with the PowerPC RISC architecture, the RMCU500 μCs have the advantage of object-code-compatible development platforms. You can use PowerPCs (and later Apple Macintoshes) to develop and partially test your embedded PowerPC code without cross-compiling to a different target architecture. Development tools for the RMCU500 family include an optimizing C compiler, a linker, and an S-record generator for ROMable code.—**Ray Weiss**

*Motorola Inc, Austin, TX. (512) 891-2000.* **Circle No. 333**

**Motorola RISC MCU 505 32-bit μC**

- 4-MHz external clock
- 25-MHz internal clock, later 40-MHz static design
- Dynamically reprogrammable clock
- 32 general-purpose registers
- On-chip double-precision FPU with 32 64-bit registers
- Multiply/accumulate DSP-like instructions
- 4-kbyte instruction cache (2-way set associative)
- 4-kbyte data SRAM
- 32-bit memory bus (16/32-bit access)
- DRAM interface with 12 chip-select signals, and zero to seven wait states
- Sleep, doze, wait power modes
- 3.3V at 40 MHz, 2.2V at 25 MHz
- 700 mW typ at 33 MHz
- 750-msec interrupt latency
- 144-pin quad flatpack
- Samples available in the fourth quarter: less than $50 (10,000)

## Intel 196 16-bit μC deploys dynamic-address/data buses

You can have it your way. If you want a multiplexed bus to save board space and memory, you can dynamically configure Intel's 8XC196 microcontroller μC to have a multiplexed external bus of 8 or 16 bits. If you want speed, you can configure the μC to have a separate data and address buses. The device is the first 196 to have a demultiplexed external bus. The bus can address up to 1 Mbyte of linear address space.

The Intel 8096/196 was the first successful 16-bit μC. Today, it still dominates the 16-bit μC market. The 196, a later version, includes a raft of peripherals. Applications include disk-drive and automotive use. It is also a favorite for motor control due to its standard and specialized peripherals. The 196 has an on-chip I/O controller called the Peripheral Transaction Server, which offloads the CPU from processing peripheral and I/O events. Instead, the peripheral transaction server transfers data to or from peripherals without forcing the CPU to process an interrupt. The server acts as a pseudo-DMA controller, stealing CPU cycles to move I/O data.

The 8XC196NP has three PWM units, which you can use to drive a motor. The motor speed is proportional to the PWM signal duty cycle; a faster motor means a larger pulse; slower speed, a smaller pulse. Each PWM has 8 bits of

**Intel 8XC196NP 16-bit μC**

- 25-MHz clock
- 1-kbyte ROM
- 1-kbyte register RAM
- 1.17-msec, 16316-bit multiply
- 2-msec 32/16-bit divide
- DRAM interface with I/O controller offloads CPU (DMA)
- Two 16-bit timer/counters
- Four high-speed capture/compare channels
- Three PWM units
- Duplex serial I/O with baud-rate generator
- 33 I/O pins
- Four external interrupts
- 5V at 25 MHz, 3.3V at 16 MHz
- 100-lead SQFP/quad flatpack
- $19.50 (2000), $16.50 ROMless
- Intel Corp, Santa Clara, CA. (800) 548-4725.


# Loral Makes a Replacement for the Versatec V80™ That Uses No Liquid Chemicals.

## NEW FROM LORAL

The Loral 9080 is a plug-compatible, exact replacement for the Versatec V80. It gives you everything you want and need in a high speed printer/plotter. With the 9080, you get clean, crisp copies every time using an environmentally-friendly dry process. No chemical inks or toners.

## EASY TO INSTALL AND USE

Installation couldn't be easier. Simply unplug the V80 and plug in the 9080. The 9080 is designed to work with all existing Versatec V80 software and hardware interfaces.

Powered by the Astro-Med Print Engine, the 9080 prints high-resolution documents at 200 dpi on fanfold or roll paper. Print Speed is 15 pages per minute. Plot speed is one inch per second. Price is under $12,000.

To order the Model 9080, call (813) 378-6984. For more information write: Loral Data Systems, P.O. Box 3041 M/S41, Sarasota, FL 34230 or call our hotline (813) 377-5590.

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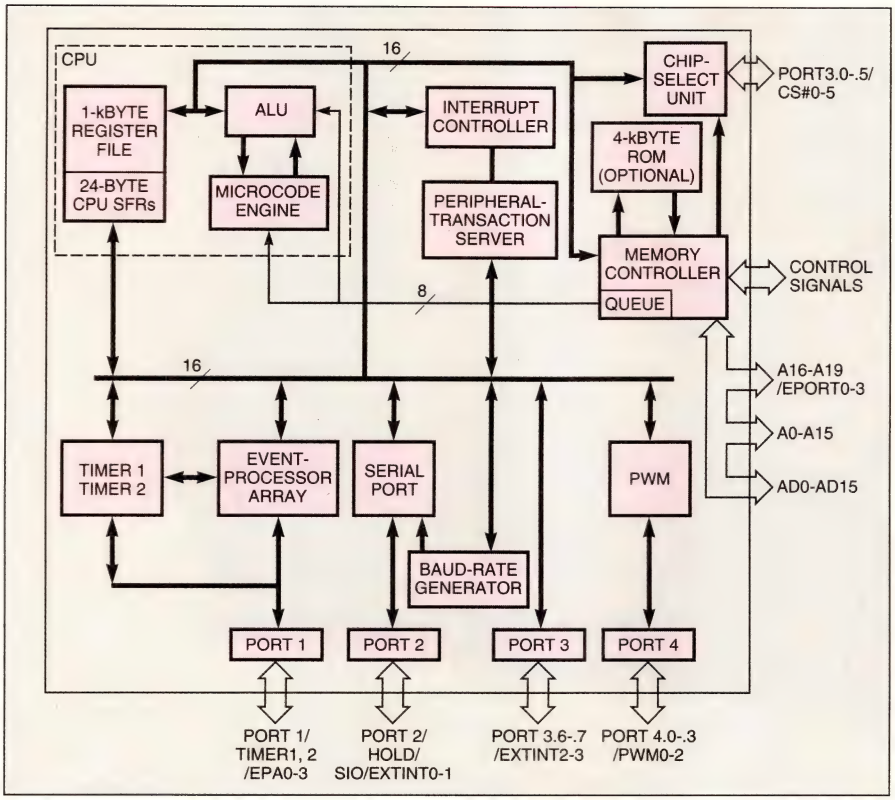


resolution and can handle 46.8 kHz (with a 24-MHz clock).

BSO Tasking supplies tools for the 196 µC. Those tools include a C compiler, a macro assembler, a locating linker, an extended floating-point library, and others. BSO also offers an in-circuit emulator for the 196. The BSO tools run on IBM PCs, and a port is under way for Unix platforms. Intel sells an evaluation board for the 8XC196NP.

**—Ray Weiss**

*BSO/Tasking, Dedham, MA. (800) 458-8276.* **Circle No. 334**

**The Intel 8XC196NP supports multiplexed and nonmultiplexed memory buses. It has a raft of on-chip peripherals, including an I/O controller, PWM units, and a serial I/O.**

# P E N

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TCP/IP

What does the future of embedded systems networking look like? Users could support all present and future networking proto-

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AppleTalk

integrated systems

# Controller offers plain and fast Ethernet combo

The IEEE's acceptance of the 100BaseX scheme for Fast Ethernet paved the way for a silicon implementation of the new 802.3U standard. That silicon is now available: the SMC91C100.

The device serves as a dual-speed CSMA/CD (carrier sense multiple access with collision detection) media access controller. It can handle 10- and 100-Mbps signals on the LAN side and can connect to 16- or 32-bit buses on the host-processor side.

For its physical-layer link, the controller can use standard CDDI or 10BaseT devices. Its media-independent interface on the 100-Mbps port will also work with 4T+ physical-layer devices when they become available.

The controller has several architectural features that simplify its use in a system. It has a flat MMU (memory-management unit) architecture connected to a 128-kbyte external memory. The flat architecture simplifies and speeds memory access relative to a page architecture.

**Dual-speed circuits allow this Ethernet controller to operate at 10 and 100 Mbps.**

The controller also boosts performance by offering a slave-only interface to the system. The reduced interface places data-flow control on the host processor, simplifying the IC's operation and reducing software overhead by eliminating bus-master arbitration.

The device uses an external serial EEPROM to hold setup information and is software-compatible with the SMC9000 Ethernet controller. The SMC91C100 comes in a 208-pin QFP and costs <$50 for the controller and a 10Base-T interface device.

**—Richard A Quinnell**

*Standard Microsystems Corp, Hauppauge, NY. (516) 435-6000.* **Circle No. 430**

# Intel CPLD combines flash memory, SRAM-based logic

Flash memory has come to complex programmable logic: Intel's Flexlogic integrates flash memory into the company's complex-PLD (CPLD) family. The iFX8160 CPLD combines eight 22V10-like configurable-function blocks (CFBs) with a chipwide global-interconnection matrix. The CPLD supports clock rates up to 83 MHz with a 10-nsec logic delay.

Flexlogic CPLDs rely on both SRAM and nonvolatile memory. The chip logic is programmed by loading the logic-defining SRAM from on-chip nonvolatile memory or from an external source. This duality makes it easy to prototype and modify logic while eliminating the need for off-chip memory to load the device on power-up.

You can define each CFB as a 22V10 look-alike or as a block of 128×10-bit SRAM. As a 22V10, the CFB contains a 60-product-term array, a product-term allocator, and 10 macrocells. Each macrocell inputs two sets of up to two product terms and can borrow more terms from adjacent cells, incorporating up to eight terms per macrocell. Additionally, the macrocells at each end of the CFB can input up to 16 product terms. Macrocell performance is independent of the number of input product terms.

**Intel flash iFX8160 Flexlogic CPLD**

- Extended 22V10 PLD architecture
- 0.6-mm CMOS
- 10-nsec logic delay
- To 83-MHz external clock
- Four chip clocks
- PCI-bus compatible, 24-mA drive
- 160 macrocells
- 16 configurable-function blocks (CFBs) (10 macrocells/CFB)
- 22V10 or 128×10-bit SRAM CFBs
- SRAM/flash-memory programmed logic
- Dynamic load or load from flash
- 100,000 to 1 million min write/erase cycles for flash memory
- Dynamic reload of one-half of a chip at a time
- 2.5-mA/MHz typ power
- 168 I/O pins, 3.3 or 5V I/O
- JTAG 1149.1
- $119 ($1000), 208-pin PQFP; $99, 15-nsec version

Each macrocell incorporates a flip-flop and an I/O pin. You can bypass the flip-flop for a pure logic function. Both the I/O pin and the logic/flip-flop signal feedback to the chipwide global interconnect. You can clock the flip-flops synchronously or asynchronously, and they can have an asynchronous set and clear. Each macrocell also incorporates a 12×12-bit signal comparator.

Intel supplies the PLDshell Plus 4.0 development tool set for Flexlogic. The software, which is free to Intel PLD customers, supports equational definitions for Intel-standard PLDs and other Flexlogic parts.**—Ray Weiss**

*Intel Corp, Santa Clara, CA. (800) 628-8686.* **Circle No. 431**

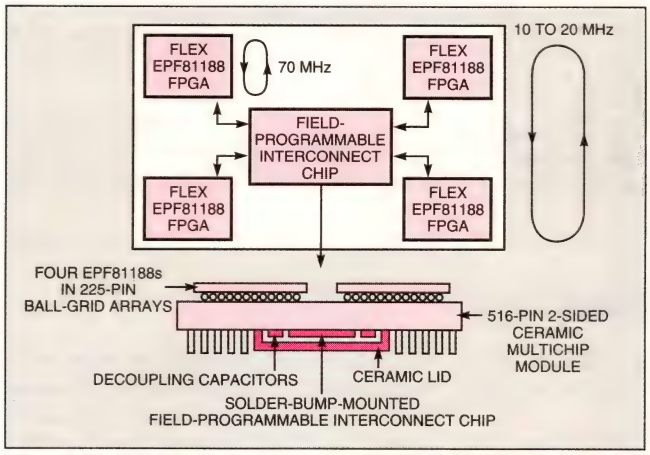
# MCM+4 FPGAs=50,000 gates, 4048 flip-flops

Sooner or later, it had to happen—the integration of multiple field-programmable gate arrays (FPGAs) on a multichip module (MCM) or a hybrid of sorts. Altera did it first, combining four Flex FPGA chips with a crossbar routing chip from Aptix on a 516-pin, 2.26×2.26-in. MCM. This combination provides the largest PLD yet available: 50,000 usable gates and 4000+ flip-flops. Signal-clock rates range from 10 to 20 MHz on the system level to 70 MHz on the FPGA chips.

The size of a large pin-grid array, the MCM can serve as a logic or ASIC-prototyping tool. It lets you download and actually run your logic, driving and receiving signals from the external world. True, you cannot run at ASIC speeds, but you can emulate or functionally execute your logic in a system. That way, you can work out functional bugs long before reaching the expensive silicon stage. Alternatively, you can use the module as a reconfigurable logic element for complex applications or as a logic-verification station.

Four Altera Flex EPF81188 FPGAs in 225-pin ball-grid-array packages mount atop the MCM. In contrast, the Aptix routing crossbar field-programmable interconnect chip (FPIC) mounts on the bottom of the MCM with flip-chip, solder bumps. The SRAM-based FPGAs and the FPIC are reprogrammable, allowing you to try out designs without burning in or removing chips.

The Flex FPGAs use on-chip SRAM to hold a logic design for execution. They have FPGA-like logic elements, each with a 4-input look-up table to map inputs into logic functions, supplemented with special carry and look-ahead logic. The logic elements, each of which has a flip-flop, are organized into groups of eight, called a logic-array block. Each logic-array block supplies fast complex-PLD-like interconnection between logic elements. These blocks, in turn, connect to a chipwide programmable interconnection with a complex PLD-like fixed delay. I/Os feed into the chipwide interconnect or to individual logic elements.




**Altera's EPF8050M integrates four EPF81188 FPGAs on a multichip module (MCM) with a crossbar routing chip. The chip routes signals between FPGAs or to external pins. The MCM fits neatly into a compact 516-pin pin-grid array.**

**Altera Flex EPF8050M FPGA/MCM**

- SRAM-based logic elements
- Four EPF81188 FPGAs
- 50,000 estimated usable gates
- 4048 logic-element flip-flops
- 70-MHz FPGA clock
- 10- to 20-MHz system clock
- Aptix field-programmable interconnect-component crossbar switch
- EPF*118 FPGA: 1008 logic elements, 126 logic-array blocks, 184 I/O pins, each pin having an I/O element with a flip-flop
- SRAM-based FPGA elements with CPLD-like routing delays
- 360 I/O pins, 516-pin pin-grid array multichip module
- $3995

Altera has extended its Max+Plus II development tool to handle the MCM with multichip partitioning and MCM/FPIC routing. Max+Plus II works from schematic; graphical; or AHDL, Verilog, or VHDL hardware-description-language inputs. Max+Plus II then partitions and synthesizes the logic and maps it into the four FPGA chips. It also routes the signals on the MCM via the FPIC chip. The tool package also includes an Aptix pin-list router, an AHDL compiler, a static-timing analyzer, and functional and timing simulators. Max+Plus II sells for $8000 and will be available by the third quarter.—**Ray Weiss**

*Altera Corp, San Jose, CA. (408) 894-7000.* **Circle No. 432**

---

**IC multiplexes video signals.** The MPC102 is a dual 2×1 signal multiplexer that distributes and routes wideband analog and digital signals. The IC comprises four identical open-loop buffer amplifiers with switching stages. Key specifications include a 210-MHz bandwidth, a 640-V/µsec slew rate, 68-dB channel crosstalk, and a ±4.6-mA (1-channel) quiescent current. Differential gain and phase errors are 0.02% and 0.02°, respectively. The device comes in 14-pin DIPs and SOICs and operates from a ±5V supply and over a temperature range of –40 to +85°C.



Prices start at $7.41 (100). **Burr-Brown Corp**, Tucson, AZ. (800) 548-6132. **Circle No. 433**

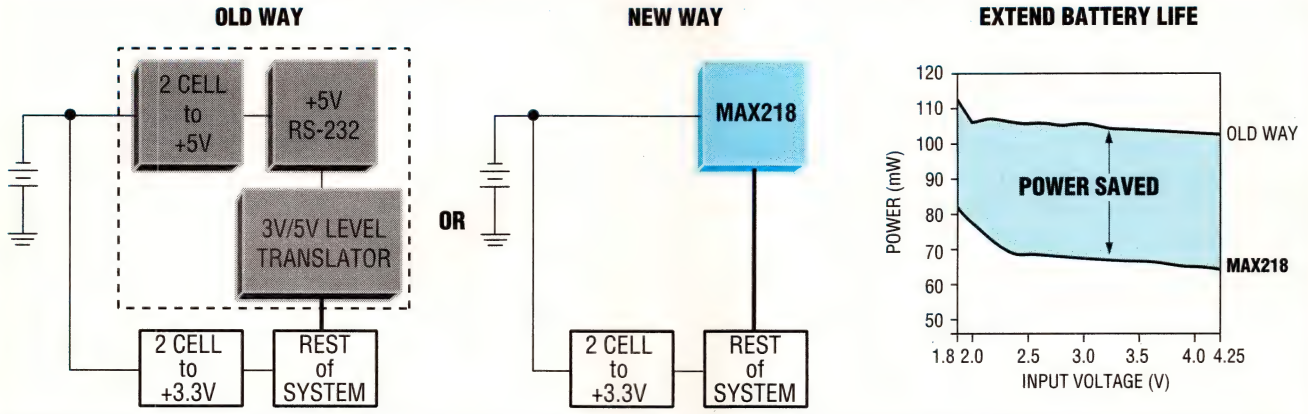
**Optical transceiver lowers cost of gigabit optical links.** The FTR-8510 transceiver combines a transmitter, a receiver, and a link controller in a 1.5×2×0.4-in. module. The device operates from 5V dc and consumes 0.8W. The transceiver transmits data streams from 100 Mbps and 1.5 Gbps using ECL or positive emitter-coupled logic (PECL) levels over standard multimode fiber lines. The optical link operates over 50/125- or 62/125-µm cable having multiple splices or connectors. The device is compatible with the ANSI X3T9.3 specification for the Fibre Channel, and it comes with duplex-SC or ST optical connectors. $660 (10). **Finisar Corp**, Menlo Park, CA (415) 364-3041. **Circle No. 434**

# 2 CELLS IN, TRUE RS-232 OUT!

## Dual Transceiver Eliminates External Regulator & Improves Efficiency

Maxim's new MAX218 dual transceiver is the first and only IC that produces true RS-232 output levels directly from 2 battery cells. And, converting from input voltages of 1.8V to 4.25V directly eliminates costly step-up converters while improving efficiency.

## Improve Efficiency & Extend Battery Life




- **1.8V to 4.25V $V_{CC}$ Operation**
- **250kbps Operation**
- **Low-Cost, Surface-Mount External Components**
- **Meets All RS-232 Specifications**
- **2 Receivers Active in Shutdown**
- **3mA Supply Current Max**

## Choose the Ideal Low Voltage RS-232 Transceiver

| PART | # Tx/Rx | Vcc RANGE (V) | SUPPLY CURRENT (mA) | Rx ACTIVE IN SHUTDOWN | DATA RATE (Kbps) |
|---|---|---|---|---|---|
| MAX212 | 3/5 | 3.00 to 3.60 | 1.2 | 5 | 250 |
| **MAX218** | **2/2** | **1.80 to 4.25** | **1.2** | **2** | **250** |
| MAX560 | 4/5 | 3.00 to 3.60 | 8 | 2 | 120 |
| MAX561 | 4/5 | 3.00 to 3.60 | 8 | 0 | 120 |
| MAX562 | 3/5 | 2.70 to 5.25 | 20 | 5 | 250 |
| MAX563 | 2/2 | 3.00 to 3.60 | 8 | 2 | 200 |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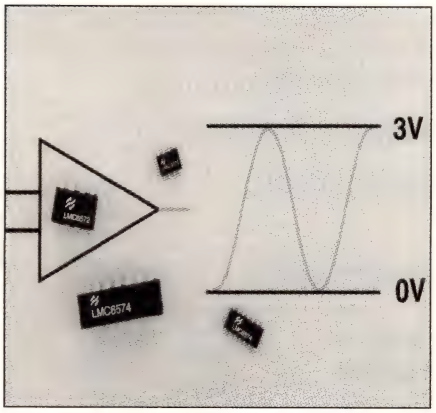
CIRCLE NO. 81

# INTEGRATED CIRCUITS

**Read-channel ICs implement partial-response/maximum-likelihood detection.** Using the company's detection implementation, the 32P4901 and 32P4902 ICs offer 80-Mbps data-transfer rates with enhanced data detection and maintain a 750-mW power dissipation. The sampled-data-detection techniques increase density by 30 to 50% over standard peak-detection recording. The ICs contain all the necessary functions for a single-chip read channel. The 4902 also offers a 4-burst servo capture for embedded applications. In OEM quantities, the devices cost <$15. **Silicon Systems**, Tustin, CA. (800) 624-8999, ext 151. **Circle No. 435**




**3V op amps swing rail to rail with high gain.** The dual LMC6572 and quad LMC6574 op amps feature guaranteed performance with 2.7 and 3V supplies, typical supply current of 40-μA/amplifier, typical and maximum input currents of 20 fA and 10 pA, respectively, and voltage gain of 120 dB when operating from 2.7V supplies. With loads of 50 kΩ, the output swings to within 20 mV of each supply rail. In 8- and 14-pin DIPs and SOICs, the dual and quad amplifiers start at $1.35 and $1.85 (1000), respectively. **National Semiconductor**, Santa Clara, CA. (408) 721-5856. **Circle No. 436**

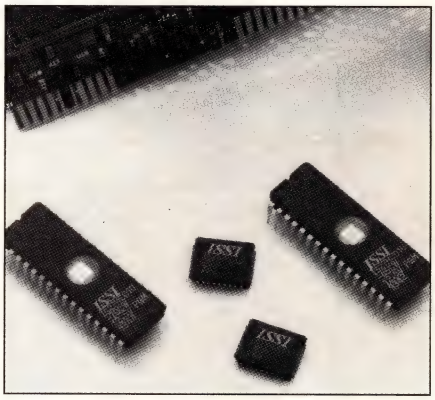
**155-Mbps clock-recovery IC operates from –40 to +85°C.** The AD802-155BR IC provides reliable clock recovery and retiming of data from fiber-optic links in a single device. The $43 (1000) device fits into a 20-pin SOIC, integrates all the necessary control logic, and requires just an external capacitor to operate. A frequency/phase-lock architecture automatically uses frequency lock for coarse acquisition and tracking, shifting to phase lock for continuous close-in, low-jitter tracking. The IC maintains the lock through a transitionless data run of up to 240 bits. **Analog Devices**, Wilmington, MA. (617) 937-1428. **Circle No. 437**

**High-speed comparators have wide input-voltage range.** The RC7341 and RC73687 dual comparators feature a maximum propagation delay of 2 nsec and an input range of –4 to 8V. The comparators have latched-data capability and ECL-compatible outputs capable of driving 50Ω terminated lines. Delay dispersion is typically 150 psec, drift is 4 psec/°C, input-offset error is 5 mV, and input bias current is typically 10 μA. The 7341 is a window comparator; the 73687 features two independent devices and is pin-compatible with the 9687. The 7341 comes in 16-pin SOICs and 28-pin plastic leaded chip carriers (PLCCs); prices start at $9.35 (1000). The 73687 comes in 16-pin SOICs and 20-pin PLCCs; starting price is $5.65. **Raytheon Co, Semiconductor Division**, Mountain View, CA. (415) 968-9211. **Circle No. 438**

**Step-up controllers are 90% efficient over 100-to-one load range.** The MAX770/771/772/773 family of dc/dc controllers provide high efficiency for 10-mA to 1A loads. The 770 through 772 accept input voltages from 2 to 16V and have preset output voltages of 5, 12, and 15V, respectively. You can also use two resistors to adjust the output voltage. These three devices comes in 8-pin DIPs and SOICs. The 773 accepts inputs from 3 to 16.5V and comes in a 14-pin DIP and SOICs. Prices start at $2.15 (1000). **Maxim Integrated Products**, Sunnyvale, CA. (408) 737-7600. **Circle No. 439**

**E1 transceiver IC reaches 2 km.** The LXT318 transceiver connects with ISDN primary-rate interfaces and network-termination units and handles cables as long as 2 km. The transceiver also incorporates selectable HD3B encoding, an adaptive equalizer, timing recovery, and a loss-of-signal processor. It needs only an external crystal for jitter attenuation and a line-coupling transformer. Cost is $27.54 (1000) for the 28-pin DIP, $28.92 for a plastic leaded chip-carrier version. **Level One Communications Inc**, Folsom, CA. (916) 985-3670. **Circle No. 440**

**IC pair provides FM LED data link.** The CXA1781N is an FM modulator that puts digital data on an LED beam using FSK modulation. A companion chip, the CXA1111P/N is an AM/FM-radio IC that decodes the LED-transmitted data. The pair operates over a 2.6 to 6V supply range and can create an IR data link that handles 60 kbps. Samples are available; the CXA1781 costs $12, and the CXA1111 costs $5. Production will begin this month, and the price will decrease to $10.50 and $1.60 (1000), respectively. **Sony Component Products Co**, Cypress, CA. (800) 288-7669. **Circle No. 441**



**1-Mbit EPROM has 30-nsec access time.** The IS27HC010 1-Mbit EPROM has a 128k×8-bit organization and is available with read-access times of 30, 35, 45, and 70 nsec. The CMOS chip is available in a 600-mil windowed ceramic package for ease of reprogrammability. The chip also comes in 32-pin plastic DIP and plastic leaded chip-carrier packages for one-time programmablity. $13 (100). **Integrated Silicon Solution Inc**, Sunnyvale, CA. (408) 733-4774. **Circle No. 442**

**Chip set provides 100-Mbyte/sec link.** The ATT DA204 and DA205 transceiver set provides a Fibre Chan-

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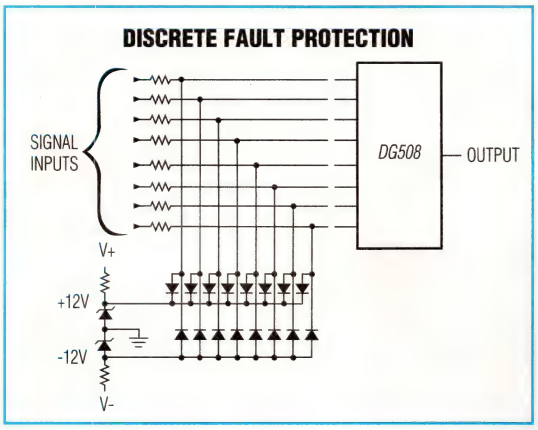
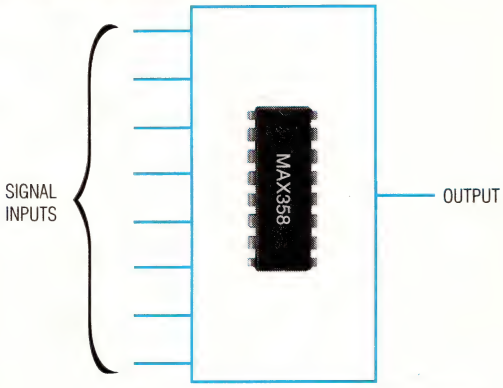
## Eliminating External Components *Reduces Cost*!




*Non-Protected DG508* $1.67
*10 Resistors, 16 Diodes, and 2 Zeners* 2.00
*Total Cost* $3.67

OR




***Eliminates External Components:***
***Total Cost $2.45***
***Cost Savings = $1.22***

| PART | UPGRADE FOR | FUNCTION (MUX) | LATCHED INPUTS | FAULT PROTECTION (V) | PRICES* ($) |
|---|---|---|---|---|---|
| MAX358 | DG508**/HI508A | 8:1 | | ±35 | 2.45 |
| MAX359 | DG509**/HI509A | 4:2 DIFF | | ±35 | 2.45 |
| MAX368 | DG528**/ADG529** | 8:1 | YES | ±35 | 3.50 |
| MAX369 | DG529**/ADG529** | 4:2 DIFF | YES | ±35 | 3.50 |
| MAX378 | HI548 | 8:1 | | ±75 | 3.50 |
| MAX379 | HI549 | 4:2 DIFF | | ±75 | 3.50 |
| MAX388 | DG528**/ADG528** | 8:1 | YES | ±100 | 4.50 |
| MAX389 | DG528**/ADG529** | 4:2 DIFF | YES | ±100 | 4.50 |

* Prices are 1000 pc., FOB USA.
** Requires external components for protection.

- **Self Protection:**
  **muxes survive ±100V overvoltage with no external components**
- **Output IC Protection:**
  **mux clamps output to ±13.5V during overvoltage**
- **Input Signal Sources Protection:**
  **only nA's of fault current with mux power ON or OFF**
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CIRCLE NO. 82

nel physical interface for 100-Mbyte/sec data transfers. The pair, fabricated in bipolar silicon, consumes <5W when operating at 5V. The devices provide retiming, transmitting, and receiving functions. The 80-pin plastic-quad-flat-pack devices will be in production by midyear and will cost $170/set (1000). **AT&T Microelectronics**, Allentown, PA. (800) 372-2447. **Circle No. 443**

**Video encoder costs <$10 in volume.** The Bt851 video encoder accepts digital video in the RGB or YCrCb color formats and converts it to baseband video, composite video, and Y/C (S-video) signals. The device includes an on-chip voltage reference and four DACs. It is pin-configurable, eliminating the need for a system processor to program the encoder. The device costs <$10 in volume and comes in a 68-pin plastic leaded chip carrier. **Brooktree Corp**, San Diego, CA. (619) 452-7580. **Circle No. 444**

**PC chip set includes VL-to-PCI bridge.** The 82C802G core logic, 82C822 PCI bridge, and 82C602 buffer ICs form the core of a 486-based PC with power-saving features. The core-logic chip contains a DRAM controller, a level-2 cache, and a VESA VL-bus interface. The bridge IC allows the computer to offer a PCI upgrade to the VL connection, providing four PCI ports and programmable mapping of PCI interrupts to ISA interrupts. The buffer IC provides power management and the real-time clock. The set costs $31 (10,000). **Opti Inc**, Santa Clara, CA. (408) 980- 8178. **Circle No. 445**

**Synchronous 1-Mbit SRAMs are as fast as 9 nsec .** The MCM67M618 and MCM67B618 1-Mbit synchronous BurstRAMs for secondary-cache applications have access times as fast as 9 nsec and a 64k×18-bit organization. The MCM67M618 operates with the PowerPC, and the MCM67B618 operates with the Pentium µP. Each version supports the specific burst-address sequence of the µP and the fastest version of each µP. The 9-nsec versions cost $55 (1000). **Motorola Inc**, Phoenix, AZ. (512) 933-4141. **Circle No. 446**

**4-Mbit SRAMs have 256k×16-bit organization.** The TC554161 4-Mbit SRAM has a 256k×16-bit organization. The device comes with access times of 85 and 100 nsec, and 70-nsec versions will be available this year. The memory has a standby power consumption of 60 µA while operating at 5V. It minimizes noise problems by using pairs of power-supply pins. The SRAM provides upper- and lower-byte controls to accommodate a µP performing 8-bit transfers. Sample price is $180. **Toshiba America Electronic Components Inc**, Irvine, CA. (714) 455-2000. **Circle No. 447**


**Codecs operate from 5 or 3V.** These 12 codecs incorporate adaptive-differential-pulse code compression, which doubles the volume of data processed in a run of code. The devices include an integrated voltage reference, employ A- and µ-Law encoding, and come in switchable versions for cellular PCM applications. The codecs come in TSOPs, and prices begin at $4.50 (1000). **Oki Semiconductor**, Sunnyvale, CA. (800) 664-6388. **Circle No. 448**

**4-kbit nonvolatile SRAM has 512×8-bit organization.** The STK-20CO4, a 4-kbit nonvolatile SRAM, is pin-compatible with Xicor's X2004 and X20C04 devices. The SRAM is organized as 512×8 bits and comes in access speeds of 30, 35, and 45 nsec. It uses Novcel technology, which combines an SRAM and an EEPROM in one memory cell. The device allows you to write or read data to the SRAM an unlimited number of times while nonvolatile data resides in the EEPROM. A control pin allows for easy transfer of data from the SRAM to the EEPROM and vice versa. A 45-nsec version costs $6.99. **Simtek Corp**, Colorado Springs, CO. (719) 531-9444. **Circle No. 449**

**Mask-programmable ROM contains 64k×16 bits.** The S631024 1-Mbit mask-programmable ROM has a 64k×16-bit organization, and its inputs and outputs are TTL-compatible. The CMOS device operates from a 5V supply and is static, so it doesn't require refresh. The device includes 3-state outputs that facilitate memory expansion by allowing the outputs to be wire-ORed. $3 (10,000). **American Microsystems Inc**, Pocatello, ID. (208) 234-6668. **Circle No. 450**

**Bidirectional buffer solves bandwidth-mismatch problems.** The FCT162701T buffer combines a 4-deep, 18-bit FIFO buffer in one direction and a read-back latch in the other. The FIFO buffer can pipeline operations, which allows a µP to run without wait states and compensate for bus-speed mismatches. Two clock-enable pins allow data-in and -out to be clocked independently. A synchronous reset flushes the FIFO buffer. The device has two octal transparent latches to minimize board space. The buffer comes in two speeds. Prices start at $3 and $5 (1000), respectively. **Integrated Device Technology Inc**, Santa Clara, CA. (800) 345-7015. **Circle No. 451**

**Chip set handles 100 VG- AnyLAN.** The Regatta 100 3-chip set provides a transceiver, a media-access controller, and a repeater using the 100 VG-AnyLAN protocol, recently adopted as IEEE 803.12. The chips allow creation of hubs and node adapters operating at 100 Mbps over Category 3 unshielded twisted-pair wire, handling Ethernet and token-ring data packets. $75 for an adapter card set; $285 for a 6-port hub set. **AT&T Microelectronics**, Allentown, PA. (800) 372-2447. **Circle No. 452**

**4-Mbit synchronous DRAM has two banks of 128k×16 bits.** The HM5241605, a 4-Mbit synchronous DRAM, offers two banks of 128k×16 bits. The DRAM has a 66-MHz burst


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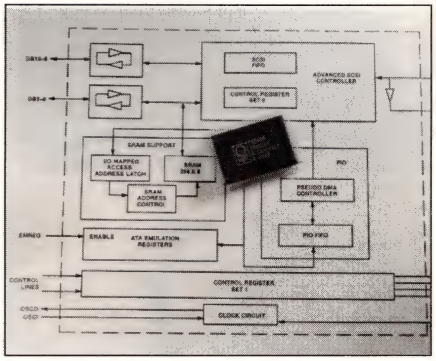
CIRCLE NO. 105

data rate and provides a bandwidth of 132 Mbytes/sec. The part has a programmable burst length as long as a full page, burst stop, byte control, auto and self refresh, and sequential or interleave burst-sequence operation. $29.50 (100). **Hitachi America Ltd, Semiconductor & IC Division**, Brisbane, CA. (800) 285-1601, ext 11. **Circle No. 453**



**SCSI adapter chip supports EISA and ISA buses.** The FAS408 is a 16-bit EISA- or ISA-bus-compatible host adapter that supports 10-Mbyte/sec Fast SCSI-2 specifications. The chip provides a glueless port, which connects directly to the AT bus, eliminating the use of a separate card slot. The device comes in a 100-lead plastic quad flatpack and includes support logic for an external BIOS ROM and a floppy controller; transceivers for direct connection to the host bus; and 24-mA drivers and receivers. $22 (1000). **QLogic Corp**, Costa Mesa, CA. (714) 438-2200. **Circle No. 454**

**Transmitter/receiver pair supports Fibre Channel.** The S2032 and S2033 transmitter/receiver pair for the ANSI X3T9.3 Fibre Channel standard handle the physical, transmission, and signaling protocols of the optical link but dispenses with the encoding and laser-drive circuits to reduce costs. The devices cost $35 to $49, depending on performance. **AMCC**, San Diego, CA. (619) 450-9333. **Circle No. 455**

**Reverse-blocking switch replaces MOSFETs and drive circuitry.** The Si9718CY allows a computer to switch from one dual-battery pack to another before battery cells are completely discharged. The IC's reverse-blocking component eliminates the parasitic diode common to standard MOSFETs, thereby reducing parts count and on-resistance. Rated at 80 mΩ and 3.5A, the device also includes charge-pump, enable, and undervoltage-lockout circuitry. The IC operates over a 6 to 18V range. In a 16-pin SOIC, the device costs $2.59 (100,000). **Siliconix**, Santa Clara, CA. (800) 554-5565, ext 18. **Circle No. 456**

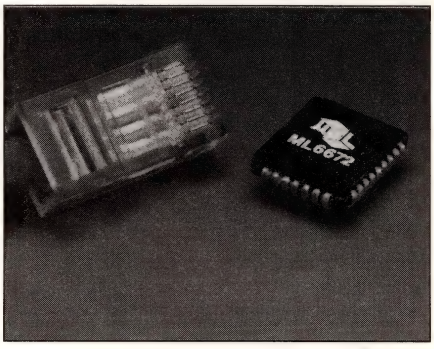
**PCI-based graphics chip offers GUI acceleration.** The DECchip 21030 for use with Pentium and Alpha AXP processors uses the PCI bus for a high-bandwidth interface. The device handles resolutions as high as 1600×1280 pixels at 24 bits and offers a 64-bit video-memory port. It also includes circuits to accelerate 3-D graphics. Price is $59.80 (5000). The vendor also plans to offer an evaluation-board kit for the chip. **Digital Equipment Corp**, Maynard, MA. (800) 332-2717. **Circle No. 457**

**HDSL transceiver goes all-digital.** The Bt8952 transceiver provides all the circuitry to adapt standard telephone wiring to a 1.5-Mbps digital data link using the HDSL protocol. The device includes 13-bit ADC and DAC circuits and 120-tap digital-adaptive echo cancellation and equalization filters. It handles various data rates, including multiples of 64 kbps, to a top speed of 1.168 kbps. Price is $37 (1000). **Brooktree Corp**, San Diego, CA. (619) 452-7580. **Circle No. 458**

**Wireless IC combines transmitter and mixer.** Combining a transmitter and a double-balanced Gilbert Cell mixer, the PMB 2206 IC converts a baseband signal into an RF carrier. The device uses two on-chip local oscillators and produces a carrier frequency as high as 2 GHz. It consumes 40 mA in operation and needs only 0.15 μA in power-down mode. Price is $5.25 (10,000). The device is available for sampling now, and the company plans production for the third quarter. **Siemens Components**, Cupertino, CA. (800) 777-4363, ext 273. **Circle No. 459**

**MOSFET drivers replace discretes.** The TC1410 to 1413 family of MOSFET drivers includes four devices with peak output currents of 0.5, 1, 2, and 3A. The CMOS devices withstand 500 mA of reverse current and negative inputs up to 5V. Typical delay time is 35 nsec, and typical supply current is 1 mA. The operating range is 4.5 to 16V. All devices are available in inverting and noninverting versions. The devices come in 8-pin DIPs and SOICs; prices range from $0.43 to $0.77 (100). **TelCom Semiconductor Inc**, Mountain View, CA. (415) 968-9241. **Circle No. 460**

**PWM controller automates power-factor correction.** The ML4824 implements current- or voltage-mode "boost"-type power-factor correction along with a synchronized current-mode PWM circuit. The IC's internal oscillator operates at 500 kHz, which enables it to improve conversion efficiency from 89 to 95%. The chip increases a computer's power-factor rating from 0.65 to 0.99. In a typical application, the IC converts 120V ac into 5V dc, but it also can produce any dc voltage from 3 to 90V. In a 16-pin plastic DIP, the IC costs $3.80 (1000). **Micro Linear Corp**, San Jose, CA. (408) 433-5200. **Circle No. 461**




**ATM chip uses copper wire.** The ML6672 chip sends and receives asynchronous-transfer-mode (ATM) protocols over unshielded twisted-pair copper wire. The copper wire replaces more expensive fiber-optic links. The allows users to share information among workstations and PCs at 155 Mbps and at distances as long as 100m. $20 (1000). **Micro Linear Corp**, San Jose, CA. (408) 433-5200. **Circle No. 460**

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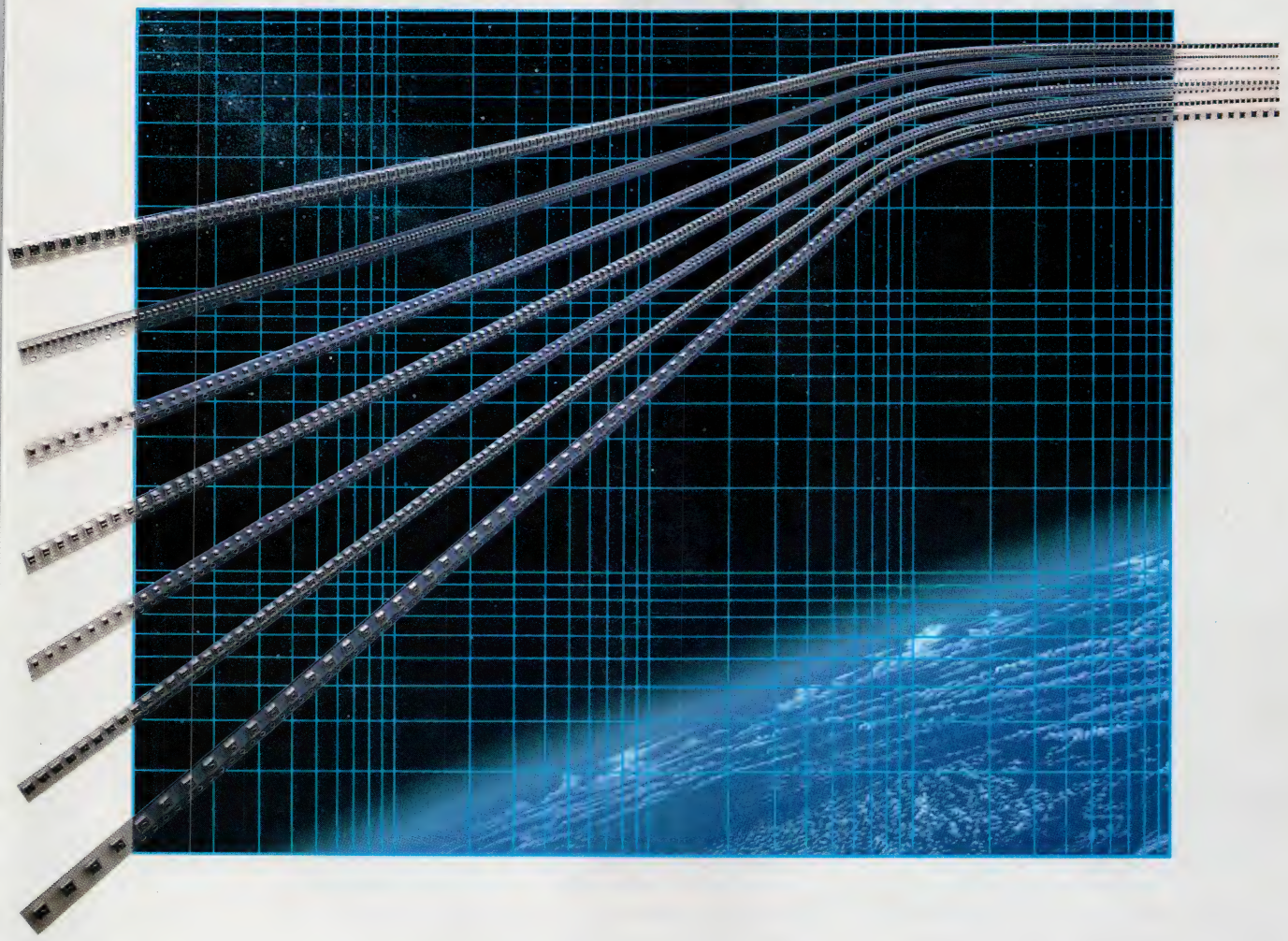

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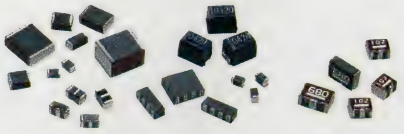

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**CIRCLE NO. 85**

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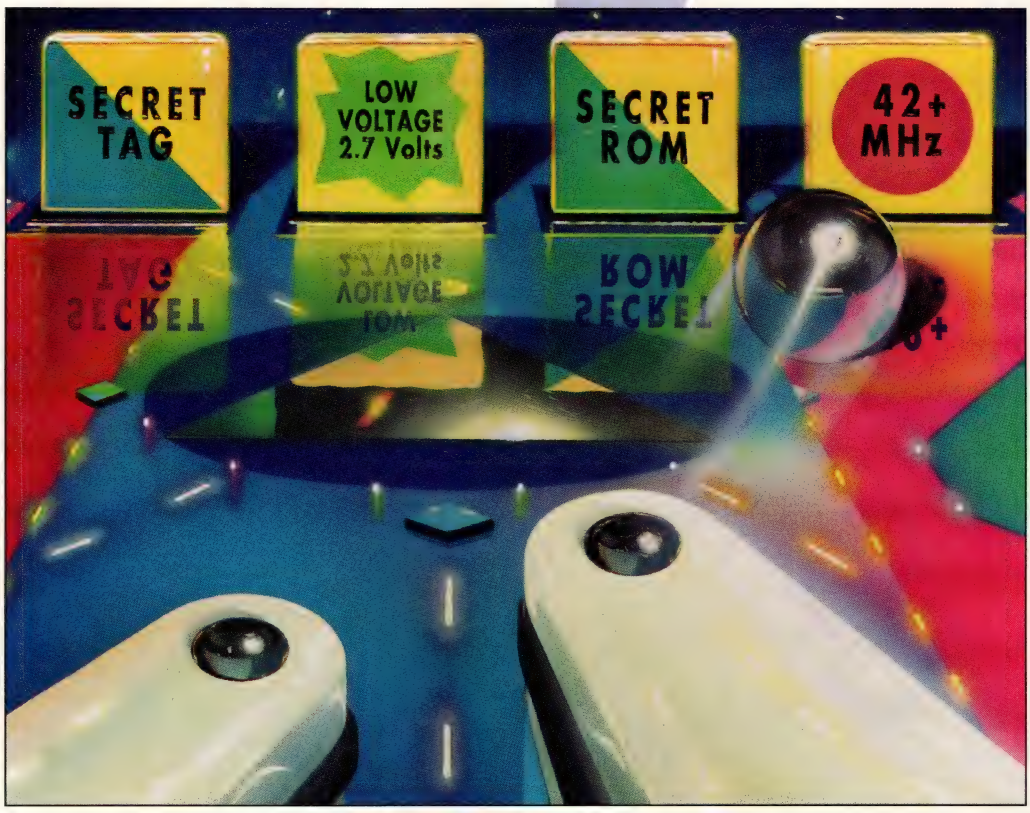


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CIRCLE NO. 107

# Boards offer upgrade to 68060

With the release of Motorola's 68060 processor, a number of vendors are planning to develop single-board computers using the device (*EDN*, "News Breaks," April 28, 1994, pg 13). Two boards—one from Heurikon Corp and the other from Motorola's Computer Group—that will enter production in July are among the first available 68060-based VME boards.

The boards have a number of common features. They both use a VME64 interface to connect the 50-MHz 68060 to the bus, and they both offer SCSI-2, Ethernet, and serial interfaces. They also offer DRAM, flash memory for reconfigurable program data, and space for PROMs. Although the features are similar, however, the two boards differ considerably in the details, as the **table** shows.

One difference is the structure of main memory. The Motorola board, designated the MVME177, has its DRAM on a 4-way-interleaved mezzanine board that can be as large as 256 Mbytes. Because it is on a separate board, the memory section can offer error-correction coding.

The Heurikon board, called the Nitro60, has its 8- or 16-Mbyte 2-way interleaved main memory on board. The device also offers a mezzanine-bus connector for its Corebus expansion structure. The mezzanine bus can hold additional memory or can provide additional I/O capability.

Another difference between the boards occurs in the area of software support. Motorola offers the Unix System/68 operating system and the VME-exec real-time development package. Heurikon offers both the VxWorks and OS-9 operating systems. It also includes an onboard monitor program and test software, residing in 512 kbytes of flash memory.

Although the 68060-based boards won't be available until midyear, designers have the opportunity of testing code on functionally identical, if slower, 68040-based boards. The MVME177 is software- and pinout-compatible with the already-available MVME147S, 162, and 167 boards. The 177 offers the same features as the MVME167, allowing users of the earlier board to make a simple board substitution to achieve three times better performance. The Nitro60 also has a pin-compatible 68040-based relative, the Nitro40 ($4995).—**Richard A Quinnell**

*Heurikon Corp, Madison, WI. (608) 831-0900.* **Circle No. 416**

*Motorola Computer Group, Tempe, AZ. (800) 759-1107, ext 77.* **Circle No. 417**

**68060-BASED VME BOARDS**

| | Motorola MVME177 | Heurikon Nitro60 |
|---|---|---|
| DRAM (Mbytes) | 4 to 256 (error corrected) | 8 to 16 |
| SRAM (kbytes) | 128 (battery backed) | 2 (nonvolatile) |
| Flash memory (Mbytes) | 4 | 4 (512 kbytes used) |
| EPROM | Two sockets | To 512 kbytes |
| SCSI-2 | 8-bit | 16-bit |
| Ethernet | Yes | Yes |
| Serial ports | Four (64 kbps) | Two (1 Mbps) |
| Parallel port | 8-bit | No |
| Base price | $4995 | $5495 |

**Expansion module adds GPIB interface.** The EXM-GPIB expansion module provides IEEE-488.2 interface capability to RadiSys computer modules with EXM expansion slots. The module offers complete IEEE-488.2 controller, talker, and listener capabilities. It operates at bus data rates greater than 1 Mbyte/sec and includes driver software for Windows and DOS. $695. **National Instruments,** Austin, TX. (512) 794-0100. **Circle No. 418**

**Power-output board offers optical isolation.** Each of the four independent output channels on the DVME-621 board is driven by a 12-bit DAC that is optically isolated from the board's data bus and powered by a fully isolated dc/dc converter. Output channels provide ±100 mA over a range of ±11V in voltage mode or can source or sink 160 mA in current mode. Settling time on the DACs is 11 µsec. The board costs $1995 and occupies a double-height 6U VME slot. **Datel Inc,** Mansfield, MA. (508) 339-3000. **Circle No. 419**

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**Module drives high-resolution flat panels.** The MiniModule/VGA-FP provides a variety of display formats, including VESA, VGA, and Hercules monochrome. The PC/104 board drives both CRT and flat-panel displays at a maximum resolution of 1024×768 pixels. It can provide 256 colors on CRTs or color LCDs and converts color to gray scale for monochrome LCDs. It includes a programmable video BIOS and onboard EEPROM to help match the board to the LCD panel's timing needs. $255 (100). **Ampro Computers Inc,** Sunnyvale, CA. (408) 522-2100. **Circle No. 420**

**Board adds SVGA to 68030 computer.** The GMS SVGA combines a local-bus SVGA module with a 68030- or 68040-based embedded computer. The board may have a VME interface or run independently. The display section drives both LCD and CRT displays simultaneously. The computer section boasts high-speed memory, allowing as much as 32 Mbytes of 2-way interleaved DRAM. From $1890. **General Micro Systems,** Rancho Cucamonga, CA. (909) 980-4863. **Circle No. 421**

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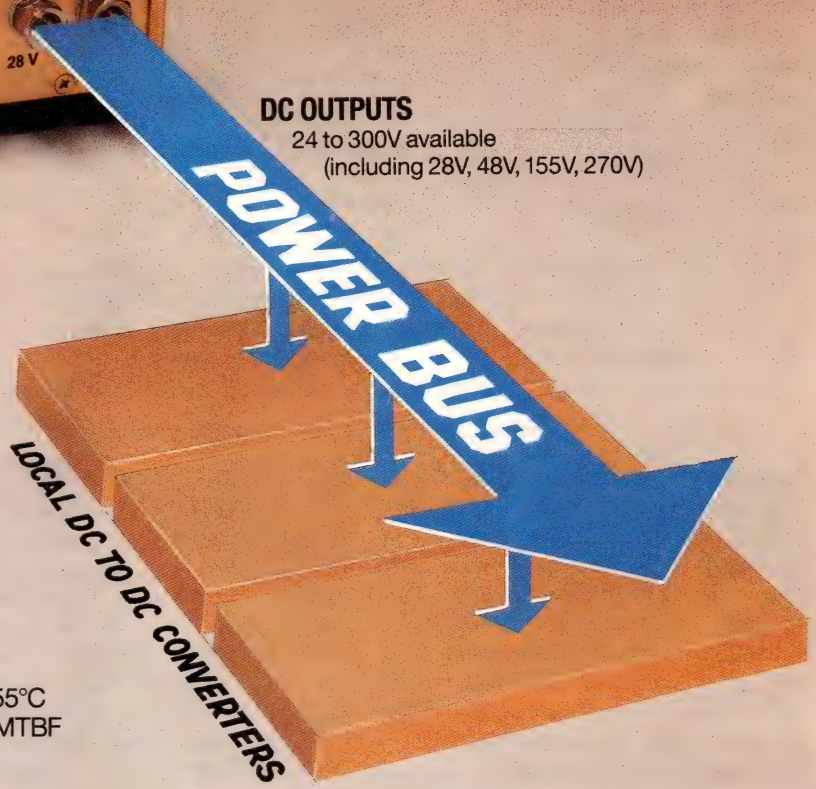


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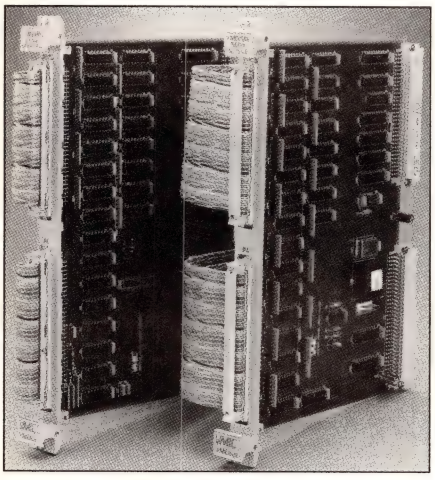
CIRCLE NO. 108

## BOARDS AND BUSES

**Adapter brings FDDI to VME64.** The PT-VME602 FDDI node adapter uses unshielded twisted-pair wire for LAN communications at 100 Mbps. The adapter provides a VME64 bus interface and offers bus buffering to decouple the LAN from the bus. The board uses a 25-MHz Mips LR33000 processor to handle network-protocol processing and to run start-up diagnostics. The board costs $2476 (100) for a single-attach FDDI interface. Dual-attach station configurations are also available. **Performance Computer,** Rochester, NY. (716) 256-0200. **Circle No. 422**



**VME repeater power-isolates slave chassis.** The VMIVME-5504L repeater link uses a single master board connected to as many as 16 slave boards with a single cable assembly. The link supports automatic slave resets on power-up or on master power-up, allowing the slave chassis to power independently of the master chassis. Master board, $750; slave, $876. Complete links, including cables, $1585 for a 10-ft link; $2277 for a 50-ft link. **VMIC,** Huntsville, AL. (205) 880-0444. **Circle No. 423**

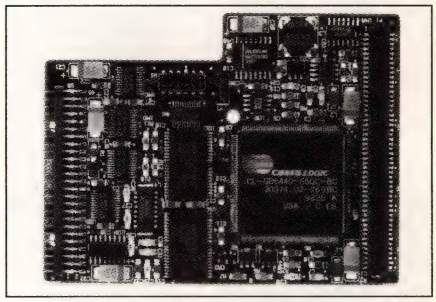
**VME boards allow PCI expansion.** The AXPvme board series operates with the Alpha AXP processor as the core CPU with a PCI bus for peripheral attachment. The AXPvme64 is a single-slot 6U board ($3495) with a 64-MHz CPU, 256-kbyte cache, and Ethernet and SCSI-2 interfaces. The AXPvme64LC, which is missing the cache and SCSI interface, is a low-cost version ($2995). The AXPvme160 is a double-height 6U board ($4995) with a 160-MHz CPU, 256-kbyte cache, and Ethernet and SCSI-2 interfaces. The boards use a 32-MHz PCI bus for all CPU-to-peripheral interfaces, including the VME interface; they offer a PCI mezzanine option card for additional I/O expansion. Samples in June; production in August. **Digital Equipment Corp,** Maynard, MA. (508) 897-5111. **Circle No. 424**

**SBus extender offers simplicity.** The Model SBus XB2-P/R board provides a passive multilayer bus extension with a signal line impedance of 75Ω. The board offers test points for monitoring each SBus signal but lacks cost-adding special features. The board costs $195 and is available with either parallel or right-angle extension connectors. **Dawn VME Products,** Fremont, CA. (510) 657-4444. **Circle No. 425**

# EDN-New Products

## BOARDS AND BUSES

**Expansion modules add to EMC line.** The embedded module computer (EMC) line has five new cards in its EXM expansion module offerings as well as two chassis. The modules are the EXM-23 LCD controller ($247), the EXM-19 24-line optoisolated digital I/O port ($179), the EXM-24 8-port RS-232C interface ($825), the EXM-28 Arcnet networking interface ($208), and the EXM-29 dual RS-422/485 port. The EMC-CH10D chassis ($213) holds 10 EXM cards and connects to a floppy disk and power supply. The EMC-CH6AT ($950) holds six EXM cards and a ISA bus card slot. **RadiSys Corp,** Beaverton, OR. (503) 646-1800.
**Circle No. 426**



**Local-bus SVGA comes to STD.** The zVid2 SVGA and flat-panel controller operates on a 486 processor's local bus to provide high-speed graphics on the ZT8902 computer board. The graphics module contains 1 Mbyte of memory and supports a CRT resolution of 1280×1024×16 bits interlaced. The module also drives most monochrome and color flat-panel displays and can be shared by several processors in a star configuration. Adapter board, $475. **Ziatech Corp,** San Luis Obispo, CA. (805) 541-0488. **Circle No. 427**

**GPS receiver fits in 3U VME card.** The DGPS is a low-power 3U VME module that contains a complete GPS receiver. The receiver can track six of eight available satellites and automatically selects among the eight to obtain the most accurate position and velocity data. Connection to the receiver data is made through a serial port. The module also provides a 1-pulse/sec timing signal accurate to 1 µsec and a universal time code. The module comes with a microstrip antenna. $1092 (OEM qty). **Dynatem,** Mission Viejo, CA. (714) 855-3235. **Circle No. 428**

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**March 28, 1994**

## ALTIUM ANNOUNCES MASTER DESIGNER 7.0
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San Jose, Calif. -- ALTIUM, an IBM Company, today announced the availability of P-CAD Master Designer 7.0 – the latest release of the premier member of P-CAD's family of printed-circuit board (PCB) design solutions for DOS, Windows, and UNIX computing environments. Designed to meet "power users" demands for maximum productivity and flexibility, Master Designer 7.0 offers multiple enhancements, including an integrated aperture table for WYSIWYG feature imaging, an enhanced on-line design rule check (DRC) capability, new auto-dimensioning features, and a more efficient user-interface.

For a limited time only, complete P-CAD PCB design solutions are now available for $1,995 – including schematic capture, layout and routing software – with upgradability of these low cost solutions to the complete range of P-CAD's Master Designer 7.0, Shapetech and Viewlogic solutions.

"Companies are looking for cost-effective design solutions that enhance engineers' ability to design PCBs quickly and accurately," said Ray Turner, EDA Marketing Manager for the P-CAD product family. "For Master Designer 7.0, we've worked closely with 'power users' to fashion a PCB design tool that's unmatched in performance and flexibility."

With this latest release, Master Designer 7.0 integrates the Gerber aperture table to provide faster, more accurate feedback to designers early in the development process when errors can be corrected more quickly and at less cost. Linked with the PCB database, the integrated aperture table provides exact flash dimensions to Master Designer 7.0's on-line design rule check (DRC), providing highly reliable clearance checking capabilities that reduce a common source of user errors in the typical PCB design project. Now, the designer sees on the screen the precise size and shape of features as they will be imaged on film for PCB fabrication.

The P-CAD product line of ALTIUM is the worldwide leader in printed-circuit board design software for PCs and workstations. With over 27,000 authorized installations worldwide, the P-CAD product line is available through value-added resellers in more than 37 countries. The productivity, reliability and flexibility of the P-CAD solutions will be demonstrated at the PCB Design Conference, March 28th to 30th, in Santa Clara, California. Seminars discussing the application of P-CAD solutions to flexcircuits, MCMs, and PCB manufacturing will be conducted at ALTIUM's P-CAD booth several times during the conference.

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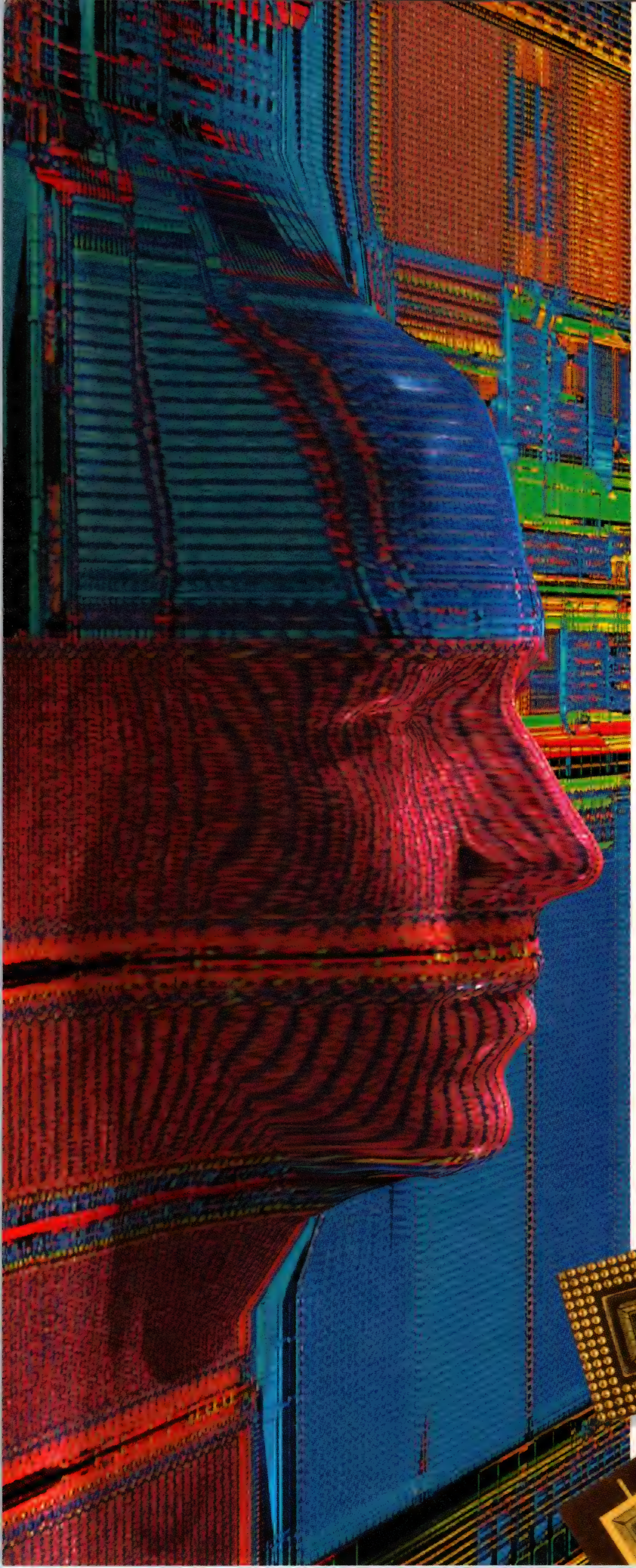

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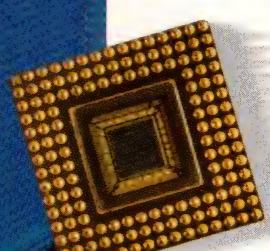

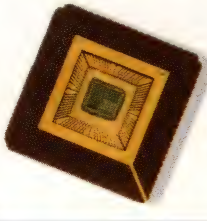

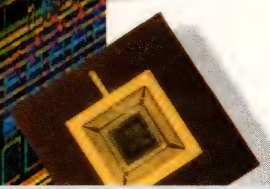

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## ELECTRONIC DESIGN AUTOMATION

# Design tools smooth synthesis-to-layout path

As part of a 5-year alliance, LSI Logic and Synopsys have been working together to keep their high-level design-automation methodology working smoothly. In theory, the concept is simple: Design at a high level using a hardware description language (HDL), verify the design using simulation, synthesize the design for your desired target ASIC, send the design off to the ASIC foundry for layout, and perform a postlayout check to ensure everything still works.

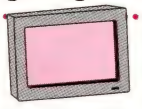
In reality, you may find timing problems during what (you hoped) would be the final postlayout timing check. Fast submicron processes coupled with large designs are making this problem painfully obvious. Although submicron designs offer short gate-propagation delays, the finer geometry increases interconnect resistance and, with it, interconnect delays. The timing problem is aggravated further by large designs, where some interconnects may be extremely long. At the postlayout stage, it's difficult to affect design timing without going back to the layout or logic-synthesis stage.

Synopsys offers an in-place optimization capability that lets you swap functionally equivalent cells for higher or lower drive versions. In-place optimization minimizes the effect on your layout and can fix small timing problems (where delays are outside the specification by only 10 to 15%).

For time delays that exceed the specification by more than 15%, the next step is to push the problem back on layout tools. Synthesis tools generate timing estimates when they synthesize logic and pass timing data forward to layout tools. Synopsys' Design Compiler provides Standard Delay File (SDF) Format timing data; LSI Logic's C-MDE Design System accepts the SDF timing information to produce a correct-by-construction, timing-driven layout.

Timing-driven layout tools can go just so far in resolving timing problems. If the logic-synthesis tool creates a design based on unrealistic interconnect delays, the layout tool probably doesn't meet timing requirements.

Floor planners provide another aid in getting from logic design to physical layout. They help you arrive at a cell placement that should minimize timing problems. However, timing problems whose roots lay in the logic-synthesis stage eventually must be resolved in logic design.



**At the postlayout stage, it's tough to affect design timing without reverting to layout or logic synthesis.**

Synopsys has attacked the timing problem in several ways. First, the company has worked with LSI Logic to use accurate nonlinear delay modeling in the synthesis process. The delay models consider the effects of input transitions and output loads on interconnect delays. LSI's wire-load models now include area and resistance information.

Second, a synthesis tool that is optimizing for area and timing may end up using too many dense fast cells, leaving insufficient routing channels. LSI Logic provides routability data in its libraries based on feedthrough per unit of cell area, and Synopsys' Design Compiler 3.1 accepts routability as a criterion for optimization by synthesis.

Third, Synopsys developed a tool called the Floorplan Manager that provides a bidirectional link between the company's logic-synthesis tools and floor planners. The tool uses cell-clustering information, for example, the data passed from LSI's floor planner via the Physical Design Exchange Format (PDEF), to calculate accurate wire delays. The tool then optimizes the design based on the physical hierarchy.

According to Synopsys, in recent tests the Floorplan Manager took a design typically having 80 to 100 postlayout-timing violations and reduced violations to fewer than 10. In one case, Floorplan Manager dropped postlayout timing violations from 300 to zero. Although not always able to eliminate design iterations, Floorplan Manager can significantly reduce iterations.

Floorplan Manager costs $40,000. LSI Logic's C-MDE Design System version 2.2, which supports timing-driven layout, is shipping now. C-MDE version 2.3 supports Floorplan Manager and should ship by July. The C-MDE Design System costs $45,000. Six Synopsys-optimized LSI Logic libraries are available now; three more will be available by the third quarter. The libraries cost $5000 per technology. Synopsys' Design Compiler costs $65,000.—**Doug Conner**

*LSI Logic, Milpitas, CA. (408) 433-8000.* **Circle No. 396**

*Synopsys Inc, Mountain View, CA. (415) 962-5000.* **Circle No. 397**

**Universal Testbench reduces time spent in VHDL test-vector preparation.** Universal Testbench eliminates the need to write VHDL code to handle test-vector input and output. The tool can automatically capture test vectors you create during interactive-simulation sessions and archive them for later use. The software can also translate stimulus files to a format compatible with IC test equipment. Universal Testbench costs $8000. **Vantage Analysis Systems Inc,** Fremont, CA. (510) 659-0901. **Circle No. 398**

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**Free design estimator compares the advantages of EPLDs.** The Logic Professor compares Xilinx EPLDs as a replacement for TTL and other PLDs. You enter the design specifications, and the software estimates the number and type of EPLDs you need to perform the task. **Xilinx Inc,** San Jose, CA. (800) 231-3386. **Circle No. 399**

**Verify FPGA designs with a VHDL simulator.** The VBAK VHDL simulator lets you back-annotate timing data to verify your field-programmable gate-array (FPGA) design. VBAK lets you put the gate-level timing information back into your VHDL model, allowing you to stay with a VHDL simulator throughout the FPGA-design process. VBAK costs $1995 for PCs and $6995 for Sun workstations. The initial release works with Xilinx FPGAs. **Topdown Design Solutions Inc,** Nashua, NH. (603) 888-8811. **Circle No 400**

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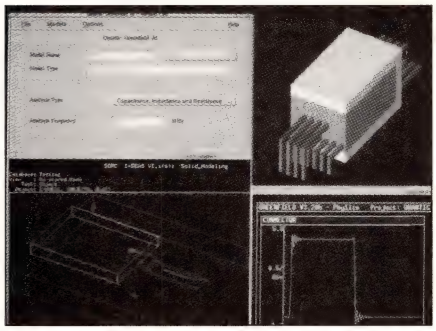
**EDA tool targets high-speed analysis problems.** The Maxwell SI Eminence software tool analyzes signal-integrity, EMI, and electromagnetic-compatibility problems. It runs on workstations and costs $49,900. The tool comes with Maxwell SI Extractor, which generates models for simulating 2- and 3-D physical interconnects. Maxwell SI Extractor alone costs $19,900. **Ansoft Corp**, Pittsburgh, PA. (412) 261-3200. **Circle No. 401**

**Module aids design of high-speed communication systems.** The Frame Relay Cloud module for the Bones product family of network-performance-analysis tools provides high-speed multiplexed data transfer in public and private networks. The parameter-based module library lets you determine the number of permanent virtual circuits and committed information rates you need to meet transaction-response requirements. The Frame Relay Cloud module costs $4000. **Comdisco Systems Inc**, Foster City, CA. (415) 574-5800. **Circle No. 402**



**Parasitics extractor creates models for 3-D structures.** The Greenfield 3d parasitics-extractor software package lets you model pc boards, connectors, cables, and IC packages by extracting the LCR parameters. The software creates a Spice model of the 3-D structure for simulation on any Spice-compatible simulator. Prices for Greenfield 3d start at $20,000. **Quantic Laboratories Inc**, Winnipeg, MB, Canada. (204) 942-4000. **Circle No. 403**

**Integrated FPGA- and PLD-design tool adds new device support.** The Synario device-independent PLD-design tool now provides synthesis and fitting for Altera's Classic, Max 5000, Max 7000, and Flex 8000 families; it also supports AMD Mach devices, including the Mach 435. Synario prices start at $2995. Prices for the Altera device kits start at $495, and the AMD Mach device kits cost $995. **Data I/O**, Redmond, WA. (206) 881-6444. **Circle No. 404**

**Verilog simulator runs on PC, Macintosh, and SPARCstation.** The VeriWell simulator, originally for PC-based Verilog simulation, is now available for Apple Macintosh and Sun SPARC computers. The company claims the simulator is compatible with Cadence's Verilog-XL simulator. VeriWell/Mac costs $1495; VeriWell/SPARC, $2995. **Wellspring Solutions Inc**, Sutton, MA. (508) 865-7271. **Circle No. 405**

**Graphics-based design tool for programmable logic.** Based on VHDL, Warp 3 uses graphical tools for design entry, timing verification and analysis, and waveform simulation. The software is built around Viewlogic's Powerview and Workview Plus design-tool frameworks. You can mix VHDL and schematic design descriptions. The software translates the entire design into VHDL and then synthesizes it to one of the company's PLDs. The software costs $4995 for use on PCs under Windows and $7495 for use on Sun workstations. **Cypress Semiconductor**, San Jose, CA. (408) 943-2600. **Circle No. 406**

**VHDL-based simulator offers analog and mixed-signal simulations.** The HDL-A VHDL-based analog behavioral simulator works with the vendor's Eldo simulator. The program lets you create analog and mixed-signal simulations. The company also offers a digital VHDL simulator (HDL-D), and you can connect the simulation to various logic simulators. HDL-A costs $30,000. **Anacad EES**, Milpitas, CA. (408) 954-0600. **Circle No. 407**

**PLD-design tool offers schematic- or text-based design.** The PLD 386+ 2.00 design tool lets you create PLD designs using the vendor's SDT 386+, OHDL hardware-design language, or a combination of the two. The tool synthesizes a design from the description and fits it into any of the more than 1000 PLDs. PLD 386+ 2.00 includes PLD fitters. $1895. **OrCAD**, Beaverton, OR. (503) 671-9500. **Circle No. 408**

**Program allows graphic creation of state diagrams.** StateCAD, running under Microsoft Windows, lets you graphically create state diagrams for PLDs and field-programmable gate arrays. The software then generates ABEL-HDL code to represent the state diagram. The software costs $995. **Data I/O**, Redmond, WA. (206) 881-6444. **Circle No. 409**

## SHORTS

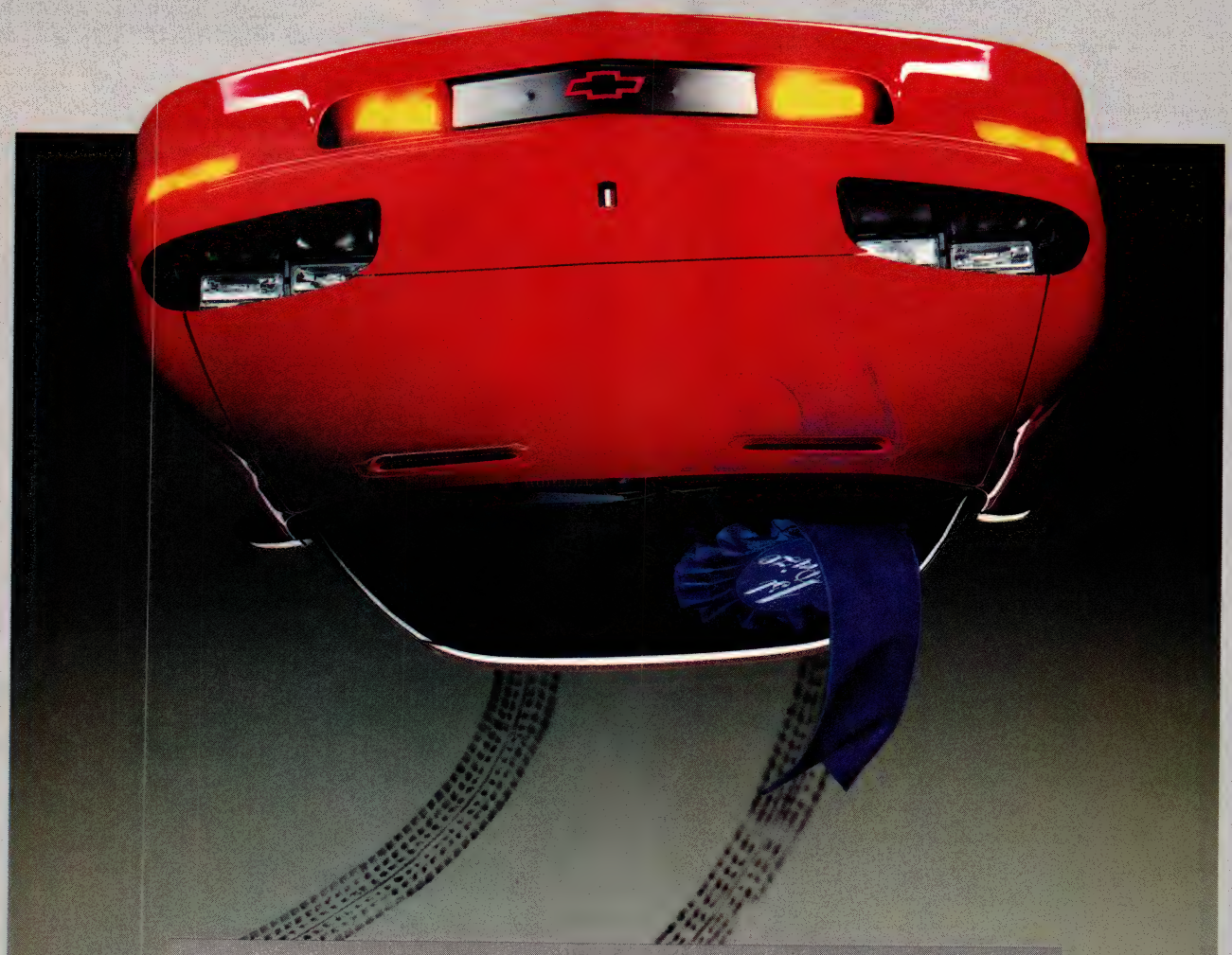
Mitsubishi supports Sunrise test tools for ASIC and embedded cell design. **Mitsubishi Electronics America Inc**, (408) 730-5900. **Circle No. 410**

Compass plans to become an OEM for Ikos's Voyager-VS VHDL simulator and integrate it with the ASIC Navigator top-down design tool for ICs. **Ikos Systems Inc**, (408) 255-4567. **Circle No. 411**

The LPKF Model 91S pc-board prototyping system mills out pc boards without using chemicals and costs $9980. **LPKF**, (503) 645-0240. **Circle No. 412**

Sunrise Test System's TestGen family of test-generation and analysis tools now provides library and foundry support for Fujitsu gate arrays. **Sunrise Test Systems Inc**, (408) 980-7600. **Circle No. 413**

Hypersignal for Windows Advanced Transmission Library provides design and analysis blocks for radio, wireline, and fiber-optic transmission systems. The library costs $1495. **Hyperception**, (214) 343-8525. **Circle No. 414**



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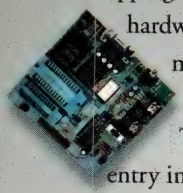



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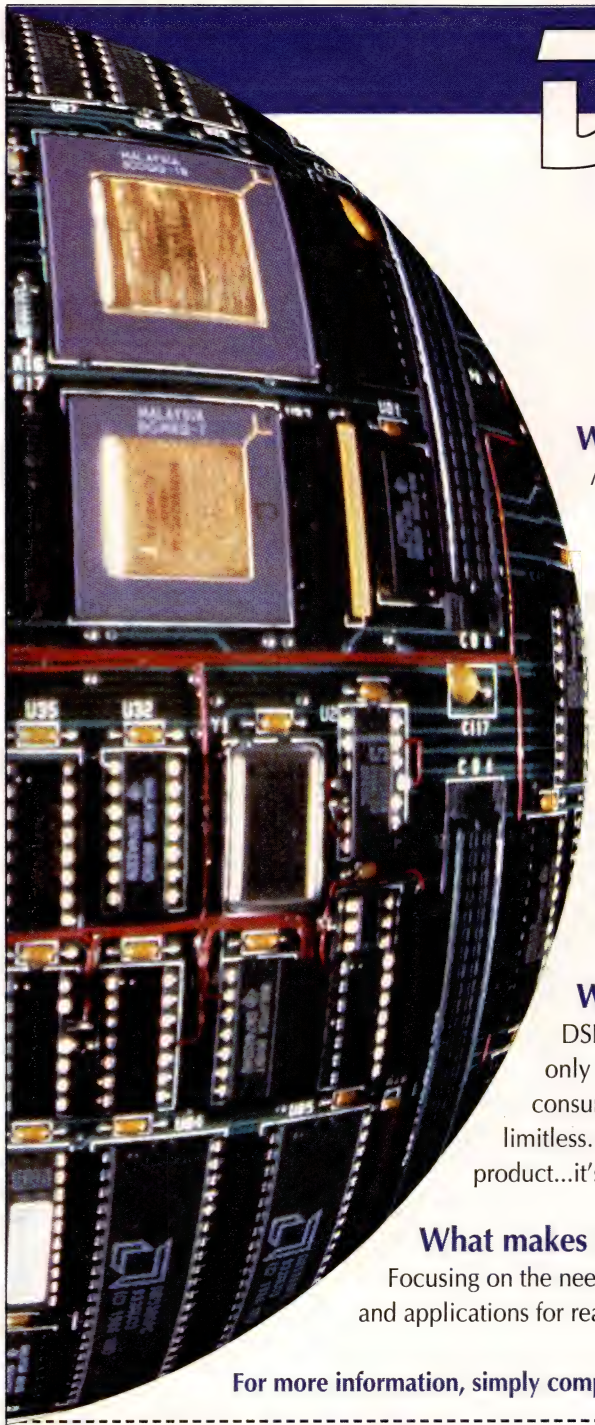

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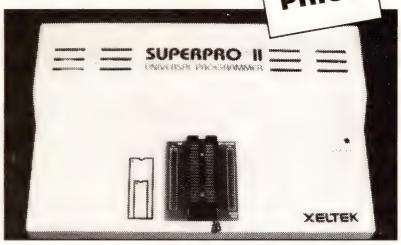


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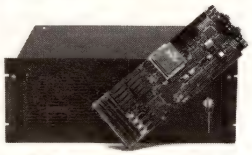

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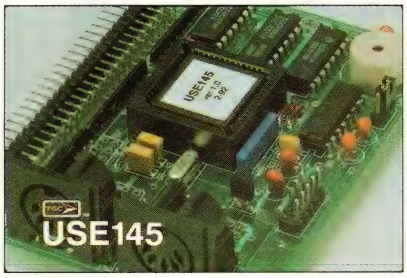


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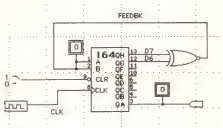

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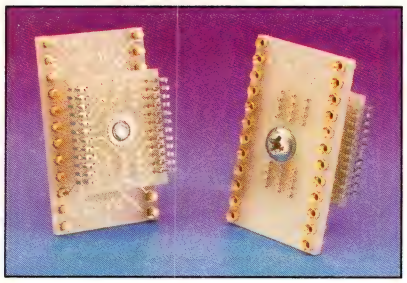

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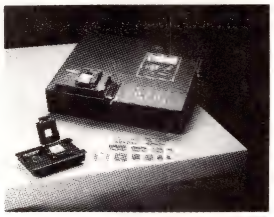

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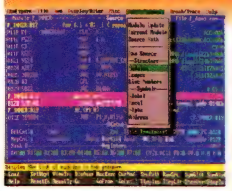

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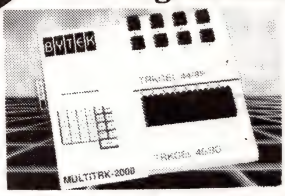


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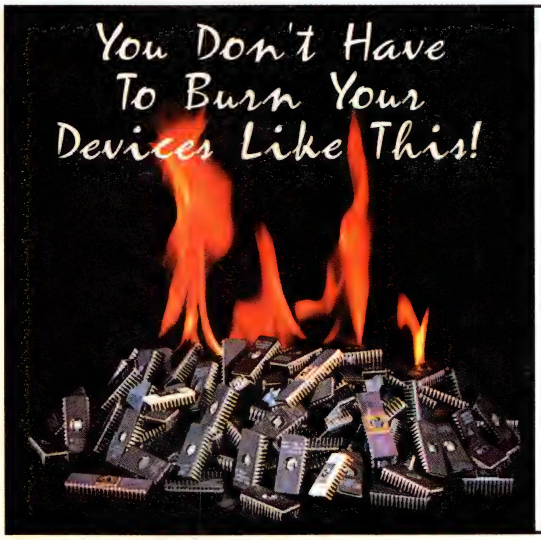


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Aero Union is located in Northern California offering a rural environment away from the smog and congestion. For confidential consideration, please send your resume and salary history to Aero Union Corp., 100 Lockhead Ave., Chico California 95926, Attention David Crivelli, Engineering Manager, EOE.



**Design Engineer**

Logic & circuit design, simulation, layout, testing & verification of new high performance digital integrated circuits. Min. MS or equiv. EE. Applications must have project/research background in s/w dev. on UNIX platforms (SUN workstations), in IC design (including mfg., testing, logic & circuit design, logic & circuit simluation, layout & verification); advanced coursework in digital & analog circuit design; knowledge of hardware & software tools required for IC design (workstations, operating systems, schematic capture, circuit simulation, logic simulation, layout & verification). $44,500/Annum. Job Site/Inter: Mississippi. Applicants clip ad and send with resume to Job: #PN1000, PO Box 641392 CYPRESS, San Jose, CA 95164-1392 no later than 5/10/94. Must have legal right to work. EOE

**IOWA MIDWEST**
**MIDWEST OPENINGS**

**RF DESIGN ENGINEERS**

MSEE/BSEE, Experience levels to 10+ years. RF/Microwave circuit design, HF to 3.0 GHz. Areas of interest are: receivers, transmitters, power amplifiers, frequency synthesizers, modulation/demodulation, spread spectrum, DSP implementation of radio functions. Multiple openings with several of my Midwest client companies.

**DON GALLAGHER, MSEE**
**Gallagher & Brei Associates**
1145 Linn Ridge Rd., Mount Vernon, IA 52314
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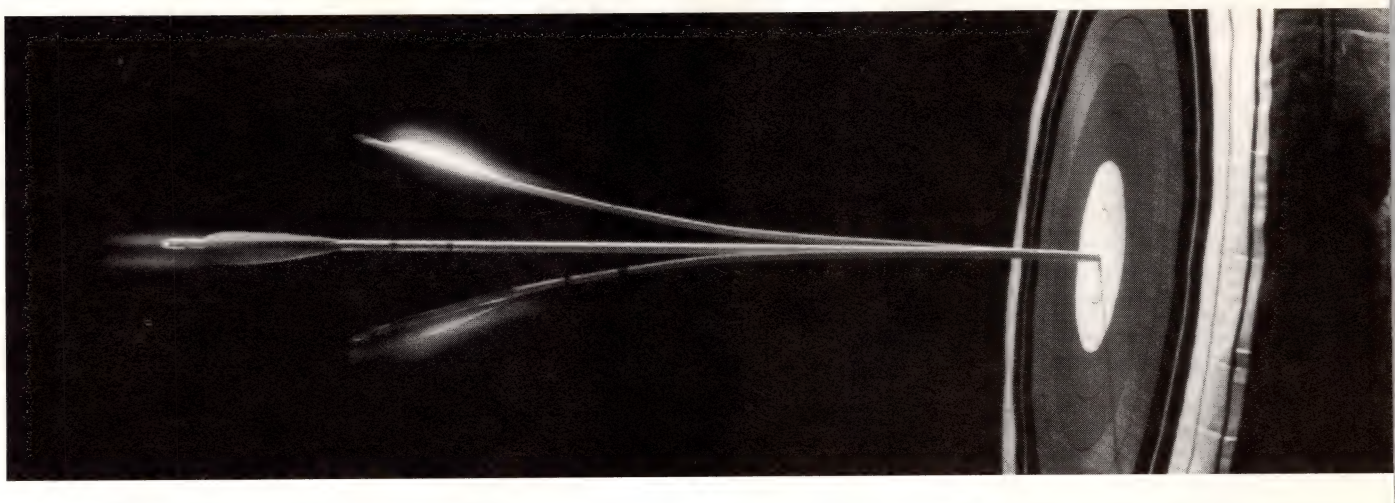

# *We've set a new goal for ourselves.*

*At Motorola Semiconductor Products Sector (SPS), excellence is simply not enough. We've already earned the enviable position of America's predominant semiconductor company by building the most diversified and advanced product line anywhere. But now, we've set our sights even higher. We're committed, completely, to a fully integrated Six Sigma And Beyond approach that ensures quality engineering at its highest level. We're creating an energizing work environment that's unequalled when it comes to involvement and advancement. And, we're taking on the world: we plan to become the best business* ***in*** *the business, anywhere.*

*If you share our sense of dedication, of determination to hit the mark higher than anyone has before, take a look at a career that's right on target. We are seeking the following professionals to join us at both our Phoenix, AZ and Austin, TX locations.*

## Phoenix Openings

*SPS's Arizona operation features new, state-of-the-art 8" wafer fab facilities in Chandler. This advanced start-up operation and our newest wafer fab facility (COM.1), being constructed in Phoenix, both utilize submicron technologies. Individuals qualified to join our team will have a related BS/MS degree and relevant experience. Opportunities exist in these and other areas:*

- ***Design Engineers***
- ***Wafer Fab Equipment Engineers and Technicians***
- ***CIM/Systems Engineers***
- ***Logic Designers***
- ***Analog Designers***
- ***Wafer Polishing Equipment Engineers***
- ***Application Systems Engineers***

*Exciting opportunities are available in Gallium Arsenide (GAAS) as we move to 6" wafer technology. Positions require related experience.*

- ***Process/Metrology Engineers***
- ***Sr. Test Engineers***
- ***Wet Process Engineers***
- ***Equipment/Process Technicians***

## Austin and Phoenix Openings

*We also seek experienced professionals with PhD degrees in Electrical Engineering, Computer Science or Computer Engineering for the following opportunities in our Sector Technology Operations in Phoenix and Austin:*

- ***Research & Development Engineers***
- ***Design Technologists***
- ***Behavioral Designers***
- ***Design Recovery Specialists***
- ***Compiler Engineers***
- ***Design Automation Engineers***
- ***Device Engineers***
- ***Microprocessor Architects***
- ***Operating Systems Engineers***
- ***Design for Test Engineers***

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*Interested candidates are invited to FAX their resumes to (602) 994-6827, or mail resumes to:* ***Motorola SPS Sourcing, Dept. SPS-544, 1438 W. Broadway Rd., Suite B100, Tempe, AZ 85282.*** *An Equal Opportunity/Affirmative Action Employer. We Welcome And Encourage Diversity In Our Workplace.*

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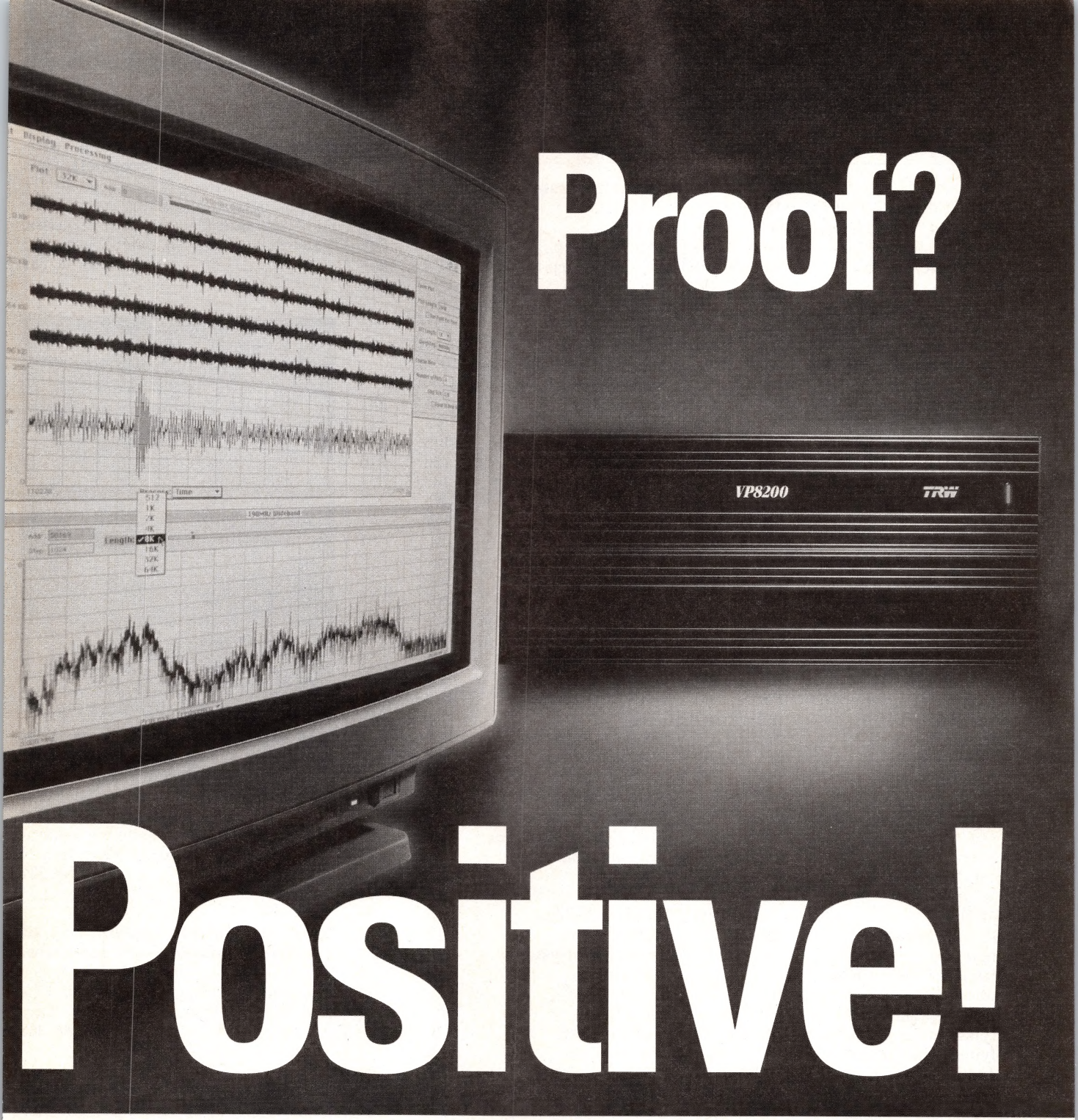


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CIRCLE NO. 113

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# EDN-Literature

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**244-pg catalog features test equipment, tools, and supplies.** This free catalog covers programmable power supplies, DMM and scope accessories, spectrum analyzers, counters, PROM programmers, function generators, and more. **Contact East Inc**, N Andover, MA. **Circle No. 382**

**Brochure details capabilities of symbolic-numeric math software.** This free 6-pg, color brochure describes Macsyma, a package available for PCs and workstations. **Macsyma Inc**, Arlington, MA. **Circle No. 383**

**Catalog of control and test I/O boards expands to 84 pages.** This free catalog is 30% larger than the previous edition. The publication covers 12 analog input and output boards, nine digital I/O boards, four communications boards, and eight input-expansion and accessory boards. **Access I/O Products**, San Diego, CA. **Circle No. 384**

**Catalog of membrane switching systems.** This catalog showcases membrane switching systems for custom applications. The 8-pg, color booklet includes product photos, mounting dimensions, technical information, specifications, options, and components. **EAO Switch Corp**, Milford, CT. **Circle No. 385**

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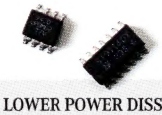

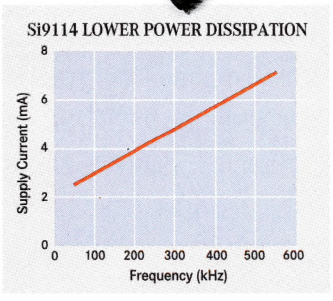


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